Design, fabrication and characterization of ion traps based on industrial microfabrication technologies

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Abstract

Ion traps are one of the most promising platforms to host a future quantum computer, as they combine the lowest error rate to date with a realistic path towards scalability. Performing useful tasks on a trapped-ion quantum computer, which have a meaningful impact in areas such as material science, logistics or security, will require hundreds or thousands of interacting ions. Although strings of more than 100 ions have been confined in linear traps, no individual control of the single ions in these devices has been achieved. Thus, scaling this technology to thousands or even more ions remains a major challenge, with one reasonable approach being the modularization of the ion trap. An important step towards realizing a large-scale trapped-ion quantum computer is the design, fabrication and characterization of microstructured ion traps. These enable complex trap designs for confining and individually controlling large numbers of single ions. Therefore, this thesis focuses on the realization of ion traps on microchips by means of industrial microfabrication technologies.

I present the fabrication and testing of a 2D ion trap array, which forms a prototype for a quantum-information processor composed of a 2D lattice of single ions. The lattice is generated by separate potential wells, each hosting one or multiple single ions. Coupling of individually trapped ions can be achieved via Coulomb interaction by reducing the distance between the lattice sites.

Furthermore, a second ion trap design was developed to face the challenge of insufficient confinement potential in surface ion traps, in which the trap electrodes reside in only one plane. An ion trap with three-dimensional architecture is presented: a surface trap created by the bottom layer of the trap is extended by a top layer with additional DC electrodes to enhance the trap depth by a factor of around ten compared to a surface trap with the same ion-electrode distance. This ion trap prototype provides a promising basis for upcoming scalable 3D ion traps with additional integrated functionality.

Zusammenfassung

Ionenfallen sind eine der vielversprechendsten Plattformen zur Umsetzung eines zukünftigen Quantencomputers, da sie die bisher niedrigste demonstrierte Fehlerrate mit einem realistischen Skalierungspfad kombinieren. Zur Durchführung nützlicher Aufgaben auf einem ionenbasierten Quantencomputer in Bereichen wie Bio- und Materialwissenschaften, Logistik oder sichere Kommunikation, werden jedoch Hunderte oder Tausende von wechselwirkenden Ionen benötigt. Obwohl bereits Ketten von mehr als 100 Ionen in linearen Fallen gespeichert wurden, konnte bisher keine Kontrolle der einzelnen Ionen in solchen Ketten erreicht werden. Die Skalierung der Technologie auf Tausende oder mehr Ionen ist deshalb eine große Herausforderung, wobei ein möglicher Ansatz die Modularisierung der Ionenfalle darstellt. Ein wichtiger Schritt auf dem Weg zur Realisierung eines skalierbaren, ionenbasierten Quantencomputers ist die Entwicklung, Herstellung und Charakterisierung von mikrostrukturierten Ionenfallen. Solche Mikrofallen ermöglichen komplexe Fallendesigns zur Speicherung einer großen Anzahl einzelner Ionen und unterstützen eine individuelle Kontrolle der gefangenen Ionen. Aus diesem Grund konzentriert sich diese Arbeit auf die Realisierung von Ionenfallen auf Mikrochips mit Hilfe industrieller Mikrofabrikationstechnologien.

Ich beschreibe die Herstellung und die Charakterisierung einer Ionenfalle bestehend aus einem zweidimensionalen Ionen-Gitter, die den Prototyp eines Quanteninformationsprozessors bildet. In dieser Ionenfalle können einzelne Ionen in separaten Potentialtöpfen gespeichert werden, die in einem zweidimensionalen Gitter angeordnet sind. Die Kopplung der einzelnen Ionen erfolgt durch Coulomb-Wechselwirkung.

Darüber hinaus wurde ein zweites Ionenfallendesign mit stärkerem Einschlusspotential als in üblichen Oberflächenfallen entwickelt. Diese Ionenfalle besitzt eine dreidimensionale Architektur: Eine untere Schicht bildet eine Oberflächenfalle, die durch eine obere Schicht mit zusätzlichen DC Elektroden erweitert wird. Diese zusätzlichen Elektroden erhöhen das Einschlusspotential im Vergleich zu einer Oberflächenfalle mit demselben Abstand zwischen Ionen und Elektroden um den Faktor zehn. Dieser Ionenfallen-Prototyp bildet eine vielversprechende Grundlage für kommende skalierbare 3D-Ionenfallen, in die zusätzliche Funktionalität wie Optik oder Elektronik integriert werden kann.

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Acronyms

AFM atomic force microscopy

AOM acousto-optical modulator

CCD charge-coupled device

CD critical dimension

CMOS complementary metal-oxide-semiconductor

CMP chemical-mechanical polishing

CSAM confocal scanning acoustic microscopy

CTE coefficient of thermal expansion

DAC digital-to-analog converter

DC direct current

DRIE deep reactive ion etching

EDX energy dispersive X-Ray analysis

EPIG electroless palladium / immersion gold

FA failure analysis

FEM finite-element method

HF hydrofluoric acid

HV high vacuum

imox inter-metal oxide

JN Johnson-Nyquist noise

KAI Kompetenzzentrum für Automobil- und Industrieelektronik

LGA land grid array

LIDE laser-induced deep etching

LPCVD low-pressure chemical vapour deposition

MEMS micro-electro-mechanical systems

NA numerical aperture

PCB printed circuit board

PDH Pound-Drever-Hall

PIEDMONS Portable Ion-Entangling Devices for Mobile-Oriented Next-generation Semiconductor-Technologies

PMT photomultiplier tube

POR process of records

QCCD quantum charge-coupled device

RF radio frequency

SEM scanning electron microscopy

SOI silicon on insulator

TEOS tetraethyl orthosilicate

TGV through-glass via

TLF two-level fluctuator

TSV through-substrate via

UHV ultra-high vacuum

via vertical interconnect access

Chapter 1

Introduction

With the increasing attention on quantum computing, the question arises what advantage this technology has over classical computing. The advantage of quantum computers is mainly given by the fast and efficient solution to special mathematical problems, such as optimization problems and the simulation of quantum systems, where classical computers quickly reach their limits. Examples for such algorithms are Shor's algorithm [1] for the factorization of large numbers, or Grover's search algorithm [2] for scanning through large sets of unstructured data. Moreover, as suggested by Richard Feynman [3] as early as 1982, such a quantum system can also be used to simulate and understand the behavior and dynamics of other quantum systems. Currently, the search for new quantum algorithms is ongoing, with potential applications in a wide range of fields, such as materials science, in the search for room-temperature superconductors [4], or life sciences, to improve the efficiency of fertilizer production [5], or to find new pharmaceuticals [6]. However, the mentioned computational advantage can only be achieved when the quantum computer system reaches a sufficient size, which is currently still a major technological challenge.

Quantum computing with trapped ions

There are various physical systems for constructing a quantum processor, such as superconducting circuits [7], trapped ions [8], photonic qubits [9], quantum dots [10], neutral atoms [11] or nuclear magnetic resonance (NMR) devices [12]. In order to assess the suitability of a technology for the development of a quantum computer, David DiVincenco [13, 14] has established the following criteria:

1. A scalable physical system formed by well-characterized qubits

2. Initialization of the qubit to a suitable state

3. Long coherence times exceeding the time necessary to perform gate operations
4. A universal set of quantum gates
5. A reliable method for detecting the qubit state

Trapped-ion quantum systems satisfy most of these criteria: The two-state qubit system is formed by two electronic states of the ion. The initialization of the qubit state is achieved by laser cooling of the motional modes and optically pumping the ion to the desired electronic state. Coherence times in the range of minutes can be achieved [15], exceeding typical gate times in the range of microseconds. Moreover, a universal set of quantum gates has been found, and these gates have already been implemented with high fidelities of $> 99.99\,\%$ for single qubit gates and $> 99.9\,\%$ for two-qubit gates [16, 17]. State-dependent fluorescence detection gives a reliable method to read out the qubit state [18]. Moreover, as an additional prerequisite, moving ions inside the trap, also referred to as *ion shuttling*, has been demonstrated for different ion trap geometries [19–21].

While most of these requirements have already been individually demonstrated, scaling the number of ions to hundreds or thousands of ions still remains one of the major challenges towards a universal trapped-ion quantum computer. Today, experiments with trapped ions are often conducted in ion traps, where the ions are trapped inside a single confining potential well [22–25]. These traps are easy to fabricate and are well suited for operation with a limited number of ions. However, trapping long strings of ions in a single potential leads to several complications: With the number of ions trapped in the same potential, also the number of motional modes increases, which hinders the spectral isolation and addressing of individual motional frequencies of the ions. This poses a challenge for the implementation of high-fidelity two-qubit gates. Furthermore, the axial confinement along the trap axis needs to be reduced for stable trapping of a long 1D ion chain, and low axial frequencies are very sensitive to heating up. Therefore, long linear ion traps are not suitable for scaling to more than 100 ions, which triggers the need for new concepts.

One solution to this problem is to divide the string of trapped ions into smaller modules in separate confining potential wells. Depending on the desired quantum operation, the ion strings are then shuttled and combined within the trap. One approach of such a modularization of the quantum register is the implementation of the quantum charge-coupled device (QCCD) architecture [26–28], which contains multiple functional trapping zones. Smaller modules of trapped ions are shuttled in between these zones to fulfill different tasks such as storage, interaction or read-out. A challenge of such an architecture is the requirement of junctions to connect multiple functional zones within

a reasonable scalable geometry in two dimensions. Besides QCCD, another approach towards a scalable trap architecture is a two dimensional trap array [29]. In such an array, single ions are trapped in individual trapping sites, forming a two-dimensional lattice. Coupling of ions in the array is achieved by reducing the inter-ion distance to allow for Coulomb interaction of the charged particles. In this approach, the ions do not have to be shuttled between different zones. In addition, simultaneous coupling between linear ion strings is possible. Figure 1.1 shows a schematic of both mentioned geometries.

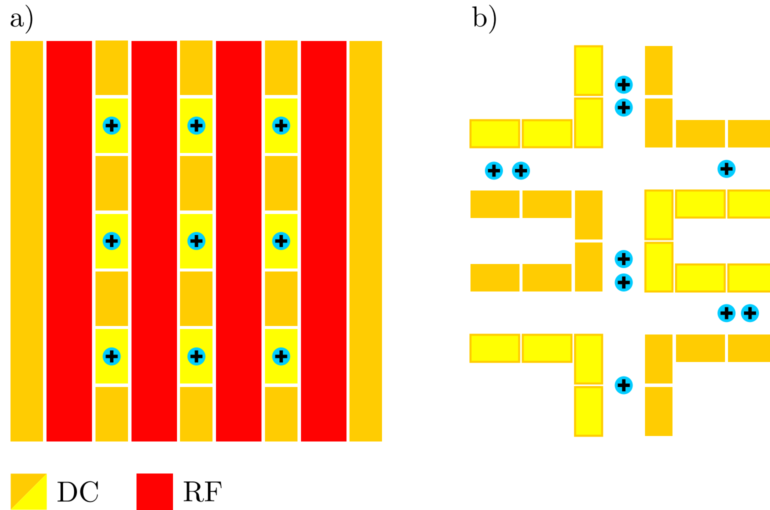

Figure 1.1: Approaches for the scaling of ion traps. a) Two-dimensional ion trap lattice array. b) QCCD architecture divided into functional zones.

Both approaches can only be realized by microfabrication of the ion trap due to the complexity of the electrode geometry. The number of required electrodes, which usually have to be individually controllable, increases with the number of trapped ions. This scaling problem can be solved by fabricating ion traps on microchips, since in this case several metal layers can be used for routing the electrical connections. Reliable and reproducible devices are required, which can be realized by an industrial fabrication based on productive standard processes from semiconductor manufacturing.

The first part of this thesis is focused on the development of a 2D ion trap array. In the developed prototype, ions are trapped in two parallel linear trap arrays, forming a two-dimensional lattice. Trapping in separate potential wells enables individual control of the single ions. By shuttling, the inter-ion distance between neighboring ions can be reduced to achieve coupling via well-to-well interactions [30–32]. A microfabrication process using a total of three metal layers separated by silicon dioxide layers is employed to achieve the routing of the 80 segmented electrodes to the bond pads at the edge of

the ion trap chip for electrical connection.

The 2D ion trap has planar electrodes, which are in principle scalable. They exhibit a low confinement potential of typically a few tens to hundreds of electronvolts, decreasing ion storage times due to background gas collisions [23, 33]. In contrast, macroscopic traps show an intrinsically much higher confinement potential generated by the symmetrical configuration of the RF electrodes. However, these traps are not scalable, since the possibilities of complex layouts are severely limited. Thus, a microstructured ion trap was developed, in which a surface trap as a bottom layer was extended with additional DC electrodes in a top layer to enhance trap depth. The increased confinement potential is generated by the effect of the top electrodes pushing the trapped ions towards the bottom electrodes, as well as by more symmetrical electric field lines in the area of the trapping site. The 3D architecture is realized by anodic wafer bonding [34] of the top and bottom wafer to a glass spacer. This trap serves as a prototype with a single trapping site, but can be scaled due to the multi-metal layer technology provided by the bottom wafer. Such a microstructured ion trap also allows for the integration of functionality in multiple layers such as electronics [35–37] or optics [38–40], which is essential for scaling beyond hundreds of controlled ions.

Finally, the concept of a 2D trap array combined with a 3D architecture for an enhanced confinement potential is presented. Basic simulations of a potential trap geometry are shown, and possible realizations through industrial manufacturing methods as well as technological challenges are described. This concept is intended to indicate a path towards large-scale trapped-ion quantum information processors.

Thesis outline

The remainder of this thesis focuses on the development, manufacturing and testing of scalable ion traps by exploiting the potential of an industrial microfabrication. Both a surface trap with 2D array geometry and a linear ion trap with 3D architecture are discussed. The thesis is structured as follows:

Chapter 2 introduces the fundamentals of ion trapping, including the working principle of Paul traps as well as experimental methods for cooling and manipulating the ion's state. **Chapter 3** gives an overview of different types of microstructured ion traps. Multiple approaches to measure and mitigate heating of the ion trap are discussed. In the following **chapter 4**, the concept and realization of a two-dimensional ion trap array based on two parallel linear strings of ions are presented. The industrial fabrication routine and electrical characterization to test the functionality are described. Moreover, the influence of different materials, used as wafer substrate and trap electrodes, on the trap performance is investigated. Simultaneous trapping and shuttling of multiple ions

is demonstrated. The next **chapter 5**, focuses on a microstructured ion trap with 3D architecture to enhance the confinement potential. The trap design, microfabrication including wafer bonding, and a quality analysis of the trap is presented. Furthermore, the performance of the trap is discussed with a basic analysis of heating rates and stray fields. In **chapter 6**, a proposal to combine the concept of the two-dimensional trap array and the hybrid ion trap with enhanced trap depth due to a 3D architecture is given. **Chapter 7** summarizes the main findings of the thesis.

Chapter 2

Fundamentals of ion trapping

In this chapter, an overview over quantum information processing in radio frequency (RF) Paul traps is given. First, the confinement and motion of ions in a radio-frequency ion trap is described. Moreover, the interaction of a trapped $^{40}Ca^{+}$ ion with laser light is discussed, which is essential for the manipulation of the ion's state and thus forms the basis for quantum operations. The last section is dedicated to the quantum optics toolbox used in the experiment, including laser cooling techniques as well as state preparation and readout methods.

2.1 Radio-frequency ion traps

In order to use ions as a basis for quantum information processing, they need to be harmonically confined in all three dimensions. Using only static electric fields, a harmonic potential

$$\phi = \frac{\phi_0}{2d^2}(\alpha x^2 + \beta y^2 + \gamma z^2), \tag{2.1}$$

is formed with d being the distance of the particle to the nearest electrode, also referred to as ion-electrode distance, which is dependent on the trap geometry. Here, the Laplace equation $\Delta\phi = 0$ must be fulfilled, so that $\alpha + \beta + \gamma = 0$. Therefore, at least one of the coefficients α, β, γ has to be negative, resulting in an anti-confinement of the particle in one direction. For this reason, a charged particle cannot be confined only by an electrostatic potential in all three dimensions [41].

To circumvent this problem, a periodic voltage can be used that creates an oscillating electric field in two dimensions [42]. Figure 2.1 shows a linear Paul trap with hyperbolically shaped trap electrodes confining the trapped ions.

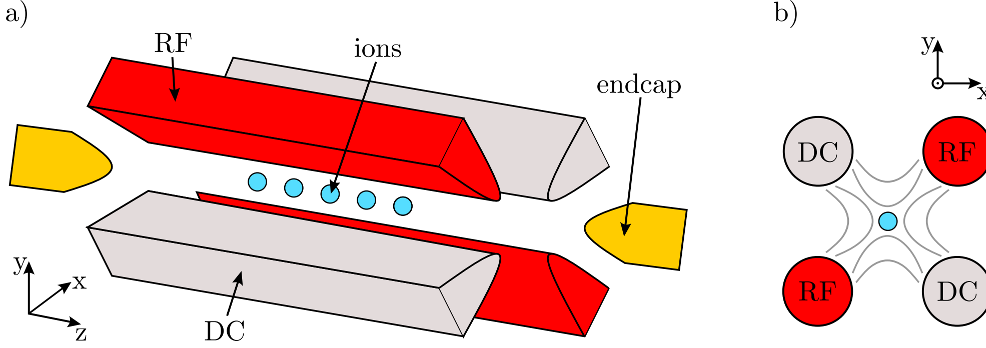

Figure 2.1: Schematic of a Paul trap. a) RF (red) and DC (gray) electrodes form a quadrupole potential that confines the ions (blue circles) in the xy-plane. Additional DC endcap electrodes (yellow) provide confinement in the third dimension. b) Cross section through a Paul trap's electrodes forming the quadrupole potential. Gray lines indicate the electric field lines confining the ion.

Applying an RF voltage of $V_{\mathrm{RF}}\cos(\Omega_{\mathrm{RF}}t)$ with amplitude V_{RF} at an RF drive frequency Ω_{RF} to the trap electrodes, which are positioned in parallel to the trap axis, generates a time-varying quadrupole potential given by

$$\phi_{\mathrm{RF}}(t) = \frac{\kappa_d V_{\mathrm{RF}}}{2d^2}(x^2 - y^2)\cos(\Omega_{\mathrm{RF}}t) \tag{2.2}$$

with the assumption of infinitely long electrodes. Here, κ_d is a dimensionless parameter related to the geometry of the trap electrodes. It defines the strength of the quadrupole potential for a certain ion-electrode distance d and trapping voltage amplitude V_{RF} [43]. As a crude simplification, dynamic trapping is realized for sufficiently fast oscillating RF fields compared to the ion's motion: the direction of the oscillating potential changes faster than the ion can escape in the direction of the anti-confinement. In a Paul trap, the RF quadrupole potential is combined with a static potential ϕ_{DC} that confines the ion in the third dimension. This static potential is generated by applying a DC voltage U_{DC} to the so-called endcap electrodes. The total potential of the ion trap is then given by

$$\begin{aligned}\phi(t) &= \phi_{\mathrm{RF}}(t) + \phi_{\mathrm{DC}} \\ &= \frac{\kappa_d V_{\mathrm{RF}}}{2d^2}(x^2 - y^2)\cos(\Omega_{\mathrm{RF}}t) + \frac{\kappa_s U_{\mathrm{DC}}}{2d^2}(2z^2 - x^2 - y^2),\end{aligned} \tag{2.3}$$

with a geometric factor κ_s, analogous to κ_d. In this electrode configuration, a direct current (DC) potential statically confines the ion in the axial (z) direction and an RF

quadrupole potential dynamically confines the ion in the radial (x-y) directions of the ion trap.

The ion's motion in a potential as defined in equation (2.3) is given by a set of differential equations; the equation of motion in the quadrupole potential is given by

$$\ddot{x}(t) = \frac{-Qx}{Md^2}\left(U_{\mathrm{DC}} + V_{\mathrm{RF}}\cos(\Omega_{\mathrm{RF}}t)\right) \tag{2.4}$$

$$\ddot{y}(t) = \frac{-Qy}{Md^2}\left(U_{\mathrm{DC}} - V_{\mathrm{RF}}\cos(\Omega_{\mathrm{RF}}t)\right), \tag{2.5}$$

where Q and M are the ion's charge and mass. These equations correspond to a special form of the Mathieu equation [43], by introducing the substitutions

$$q = \frac{2QV_{\mathrm{RF}}}{Md^2\Omega_{\mathrm{RF}}^2} \quad \text{and} \quad a = \frac{4QU_{\mathrm{DC}}}{Md^2\Omega_{\mathrm{RF}}^2}, \tag{2.6}$$

also referred to as *stability parameters*. In the limit of $|a|, q^2 \ll 1$, stable solutions of the ion motion can be derived [44], leading to an approximate ion motion of

$$x, y(t) \propto \cos(\omega_r t)\left[1 - \frac{q}{2}\cos(\Omega_{\mathrm{RF}}t)\right] \tag{2.7}$$

with the radial frequency ω_r of the ion. The stable regime of the ion motion is found for values $q < 0.908$ in linear Paul traps [44]. Note, that stability conditions have to be satisfied in all three dimensions simultaneously. For the ion traps presented in this work, stability parameters $q \leq 0.4$ are chosen, as instabilities in the ion motion arise at higher values of q [45].

One method to describe the ion's motion is the *pseudopotential approximation*. Here, the ion's motion is understood as an oscillation caused by a ponderomotive potential induced by the RF field, resulting in the pseudopotential given by

$$U_{\mathrm{ps}} = \frac{Q^2}{4M\Omega_{\mathrm{RF}}^2}|\nabla\phi_{\mathrm{eff}}(x, y, z)|^2, \tag{2.8}$$

where ϕ_{eff} relates to the RF quadrupole potential from equation (2.2) for $\cos(\Omega_{\mathrm{RF}}t) = 1$. This corresponds to a pseudopotential of

$$U_{\mathrm{ps}} = \frac{Q^2 V_{\mathrm{RF}}\kappa_d^2}{M\Omega_{\mathrm{RF}}^2 d^4}(x^2 + y^2). \tag{2.9}$$

The ion's motion at the radial frequency ω_r is then approximately given by

$$\omega_r = \frac{\Omega_{\mathrm{RF}}}{2}\sqrt{a + \frac{q}{2}}, \tag{2.10}$$

and is also called *secular motion*. The secular motion is modulated by the RF drive frequency, resulting in a fast oscillation, the so-called *micromotion*. Micromotion occurs

in trap areas where the RF field is not zero, e.g. due to poorly aligned electrodes, defects, or in junctions. Note, that micromotion can also occur in perfectly aligned ion traps. Excess micromotion is usually caused by stray electric fields that push the ion out of the potential minimum. To compensate for excess micromotion, additional static electric fields are used to control the ion's position in the trap. Moreover, the ion's harmonic motion in the static potential along the trap axis is described by the axial frequency

$$\omega_z = \frac{2Q\kappa_s U_{\mathrm{DC}}}{Md^2}. \tag{2.11}$$

The pseudopotential approximation was used to simulate the ion traps presented in this thesis, since it enables a quasi-static simulation of the dynamic trap confinement via the RF field amplitudes.

2.2 The calcium ion

Multiple types of ion species have proven to be a reasonable basis for quantum information processing with trapped ions [46]. An important requirement to the ion species is a simple energy structure that allows for the use of common laser cooling methods [33]. Moreover, it is also advantageous if solid-state laser systems are available for all relevant optical transitions. The ion traps described in this thesis are designed for trapping calcium ions. Calcium is in the second main group of the periodic system, the alkaline earth metals. The $^{40}\mathrm{Ca}^+$ isotope has only one valence electron in the outer shell and has no nuclear spin.

The ground state of the $^{40}\mathrm{Ca}^+$ ion is the $4S_{1/2}$ state. All relevant dipole-allowed and quadrupole-allowed transitions of the level structure are depicted in figure 2.2. The dipole-forbidden transition from the $4S_{1/2}$ to the $3D_{5/2}$ state is driven through a quadrupole transition ($\Delta l = +2$) with narrow bandwidth $\lambda_{\mathrm{qubit}} = 729\,\mathrm{nm}$ laser light. Due to its long lifetime of around 1 s [47], which is the ultimate limit for decoherence, the $3D_{5/2}$ state is chosen as the qubit state. This lifetime is sufficient for the target quantum operations [33]. Applying laser light with 854 nm wavelength pumps population back to the ground state via the $4P_{3/2}$ state, which is used for quenching the lifetime of the qubit state during state initialization as well as for sideband cooling. The $4P_{1/2}$ state with a decay time of 10 ns [48] is used for detection and laser cooling of the ion with a transition frequency of $\lambda_{\mathrm{cooling}} = 397\,\mathrm{nm}$. Depletion of the long-lived $3D_{3/2}$ state is implemented through repumping to the $4P_{1/2}$ state with 866 nm laser light. Subsequently, the ion will decay with high probability to the ground state for reinitialization.

When applying an external magnetic field of a few Gauss to define the quantization

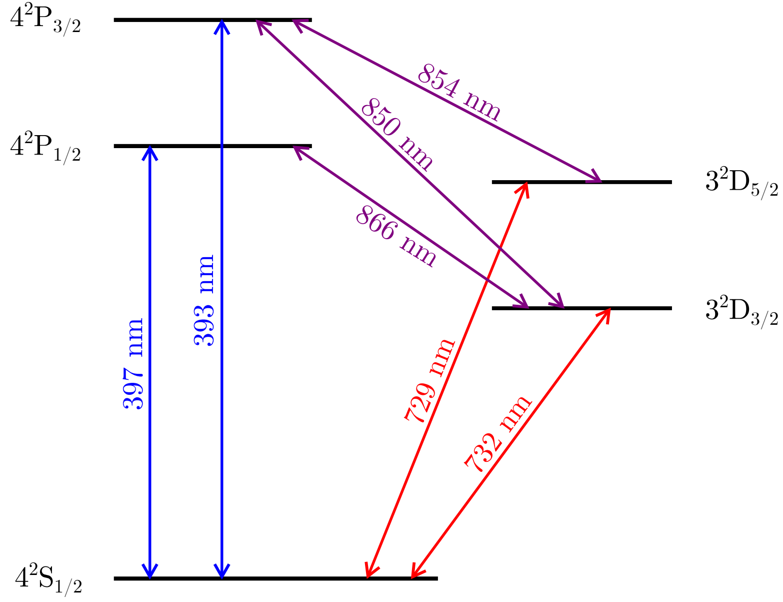

Figure 2.2: Energy levels of the Ca ion. Transitions are marked with corresponding wavelengths. Blue lasers are used for cooling and detection, red lasers for manipulation and lasers colored in purple for repumping.

axis of the ion trap, the degeneracy of the energy levels in the fine structure is lifted. For the $4S_{1/2} \rightarrow 3D_{5/2}$ transition the splitting due to the Zeeman effect results in 10 resolved quadrupole transitions with $m_j = (-J, -J+1, ..., +J)$, as shown in figure 2.3. Three of these transitions are of interest for the experiment:

- $4S_{1/2}(m_j = -1/2) \rightarrow 3D_{5/2}(m_j = -1/2)$ defines the qubit transition
- $4S_{1/2}(m_j = -1/2) \rightarrow 3D_{5/2}(m_j = -5/2)$ is used for sideband cooling (further details will follow in section 2.4.2)
- $4S_{1/2}(m_j = 1/2) \rightarrow 3D_{5/2}(m_j = 3/2)$ to apply optical pumping.

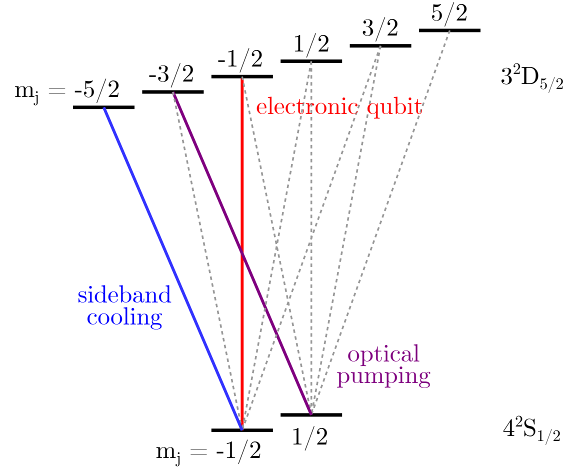

Figure 2.3: Zeeman sublevels of the Ca ion for the $4S_{1/2}$ and the $3D_{5/2}$ states. Highlighted transitions are used for sideband cooling (blue), optical pumping (purple) and the qubit encoding (red).

2.3 Ion-laser interaction

To define the two-level system presenting an optical qubit, two states of the calcium ion can be used. The ion's state can be in a superposition of the ground state $|\mathrm{g}\rangle$ given by $4S_{1/2}$ and the excited qubit state $|\mathrm{e}\rangle$ given by $3D_{5/2}$ as described by

$$\psi = \alpha|\mathrm{g}\rangle + \beta|\mathrm{e}\rangle \tag{2.12}$$

where the complex numbers α and β satisfy the condition $|\alpha|^2 + |\beta|^2 = 1$. The Hamiltonian of the system is then given by

$$H = H_a + H_m + H_i, \tag{2.13}$$

where H_a describes the electronic state of the ion, H_m is associated to the ion's motion in the harmonic trap potential, and H_i represents the interaction of the ion with the light-field. The atomic Hamiltonian is given by

$$H_a = \frac{\hbar\omega_0}{2}\left(|g\rangle\langle g| - |e\rangle\langle e|\right) \tag{2.14}$$

with the energy difference $\hbar\omega_0$ between the ground state and the excited state. Using the Pauli spin matrices [44], equation (2.14) can be written as

$$H_a = \frac{\hbar\omega_0}{2}\sigma_z. \tag{2.15}$$

The ion's motion in the harmonic potential with the motional secular frequency ω_m is given by

$$H_m = \hbar\omega_m \left(\frac{1}{2} + a^\dagger a\right) \tag{2.16}$$

with the creation and annihilation operators $a^\dagger$ and a of the harmonic oscillator, respectively.

The optical qubit is controlled by a manipulation of the ion's state by resonant laser light. An electromagnetic wave is defined as

$$E(z,t) = E_0 \left[e^{i(kz-\omega_l t+\phi)} + c.c.\right] \epsilon \tag{2.17}$$

with the amplitude E_0, the phase ϕ and frequency ω_l of the laser, propagating along the direction k. The interaction Hamiltonian of the ion with the light field is then given by

$$H_i = \frac{1}{2}\hbar\Omega \left(\sigma^+ + \sigma^-\right) \left(e^{i(kz-\omega_l t+\phi)} + e^{-i(kz-\omega_l t+\phi)}\right) \tag{2.18}$$

with $\sigma^\pm = \dfrac{\sigma_x \pm i\sigma_y}{2}$ [44]. The parameter Ω denotes the *Rabi frequency*, defining the coupling strength of the ion to the light field. In case of a quadrupole transition, where a metastable state is coupled to the electronic ground state of the ion, the interaction is described by the coupling of the electric-quadrupolar moment $\widehat{Q}$ to the gradient of the electromagnetic field [49]

$$H_i = \widehat{Q}\nabla E(t). \tag{2.19}$$

After transformation to the interaction picture and using the rotating wave approximation, equation (2.18) can be written as

$$H_i = \frac{1}{2}\hbar\Omega \left(\sigma^+ e^{i\eta(\tilde{a}+\tilde{a}^\dagger)} e^{-i\Delta t} + \sigma^- e^{-i\eta(\tilde{a}+\tilde{a}^\dagger)} e^{i\Delta t}\right) \tag{2.20}$$

with the detuning of the laser with respect to the transition frequency $\Delta = \omega_l - \omega_0$ and introducing the transformations $z = \eta(a + a^\dagger)$ and $\tilde{a} = ae^{-i\omega_0 t}$. The *Lamb-Dicke parameter* η is given by

$$\eta = k\sqrt{\frac{\hbar}{2M\omega_0}}. \tag{2.21}$$

Dependent on the specific detuning Δ of the laser, different motional states are coupled when driving the transition between the ground state $|\mathrm{g}\rangle$ and the excited state $|\mathrm{e}\rangle$, described by $|\mathrm{g,n}\rangle \leftrightarrow |\mathrm{e,m}\rangle$. The coupling strength of a transition can be determined by the Rabi frequency, defined as [49]

$$\Omega_{n,m} = \Omega_{m,n} = \Omega_0 |\langle n| e^{i\eta(a+a^\dagger)} |m\rangle|. \tag{2.22}$$

When the ion is cooled to the Lamb-Dicke regime, defined as $\eta^2(2n+1) \ll 1$, the interaction Hamiltonian can be further simplified and three resonances are identified [44]: if the motional state does not change, a carrier transition is observed, and the interaction Hamiltonian is given by

$$H_{\text{car}} = \frac{1}{2}\hbar\Omega \left(\sigma^+ e^{i\phi} + \sigma^- e^{-i\phi}\right). \tag{2.23}$$

If the ion is in the initial state $|g|$ and the motional state increases (decreases), a so-called blue (red) sideband transition takes place, as depicted in figure 2.4. The interaction Hamiltonian then takes the form

$$H_{\text{bsb}} = \frac{1}{2}\hbar\Omega\eta \left(a^\dagger \sigma^+ e^{i\phi} + a\sigma^- e^{-i\phi}\right) \tag{2.24}$$

$$H_{\text{rsb}} = \frac{1}{2}\hbar\Omega\eta \left(a\sigma^+ e^{i\phi} + a^\dagger \sigma^- e^{-i\phi}\right) \tag{2.25}$$

for the blue and red sideband transition, respectively.

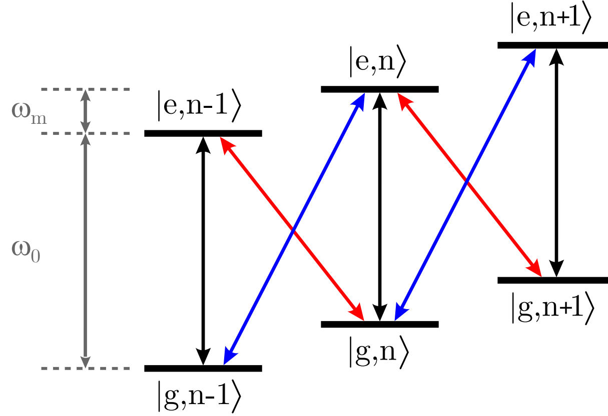

Figure 2.4: Carrier and motional sidebands of the quadrupole transition. The carrier transition (black arrows) does not change the motional state of the ion, whereas a blue sideband transition (blue arrows) reduces and a red sideband transition (red arrows) increases the motional quantum number by one phonon when driving the $|e\rangle \rightarrow |g\rangle$ transition.

2.4 Cooling, initialization and detection

A requirement for successful quantum operations is cooling the ion close to the motional ground state by laser cooling. The cooling process for a trapped $^{40}Ca^+$ ion contains two

steps: first, the motional quantum number $\overline{n}$ is reduced by Doppler cooling to around $\overline{n} = 10$, reaching the Lamb-Dicke regime. Second, resolved sideband cooling is employed to further cool the ion close to its motional ground state.

This section is dedicated to the experimental methods used in the experiment for cooling the ion, preparing the ion in the desired ground state, also referred to as state initialization, and detecting the ion's internal state.

2.4.1 Doppler cooling

The first cooling method facilitated in the experiment is Doppler cooling [50]. A red-detuned laser with 397 nm wavelength is guided towards the ion, driving the $4S_{1/2} \rightarrow 4P_{1/2}$ transition. Due to the Doppler effect, the ion preferentially absorbs a photon when it is moving towards the laser beam. When absorbing a photon, it gains momentum along the laser direction and thus gets decelerated in this direction. The following spontaneous emission of a photon occurs in arbitrary direction, leading to a random walk in momentum space. This results in a decrease of the ion's motional state during photon absorption for irradiation with red-detuned laser light, and heating for blue-detuned laser light. Due to the random photon emission, Doppler cooling has a certain limit (Doppler limit), giving a minimum temperature achievable with this technique. With an optimal red-detuning of the Doppler cooling laser of $-\frac{\Gamma}{2}$ [44], the minimum mean phonon number [50] is given by

$$\overline{n} = \frac{\Gamma}{2\omega_m}. \tag{2.26}$$

Since there is a non-negligible probability of $\sim 6\,\%$ [51] of the ion to spontaneously decay into the $D_{3/2}$ state, a 866 nm repumping laser is used to pump population back to the $P_{1/2}$ state, thus realizing a closed cooling cycle. In order to cool the ion in all motional modes, the cooling laser needs to have a component in parallel to each of the three trap axes.

2.4.2 Sideband cooling

Below the Doppler cooling limit, resolved sideband cooling is used to further reduce the motional quantum number [52]. As a requirement, the ion has to be cooled to the Lamb-Dicke regime and sidebands need to be resolved. A laser pulse of the 729 nm qubit laser with a detuning of $\delta = -\omega_\mathrm{m}$ is applied. The detuned laser addresses the first red sideband and drives the $|\mathrm{g}, n\rangle \rightarrow |\mathrm{e}, n-1\rangle$ transition. This decreases the motional quantum number by one phonon. Repeating the cooling cycle multiple times decreases the motional quantum number of the ion close to the motional ground state

[53]. To increase the cooling rate, a resonant 854 nm repumping laser is used to couple the metastable $D_{5/2}$ state to the short living $P_{3/2}$ state. This state decays with high probability via the carrier transition to the $S_{1/2}$ ground state. The sideband cooling process is sketched in figure 2.5 for visualization.

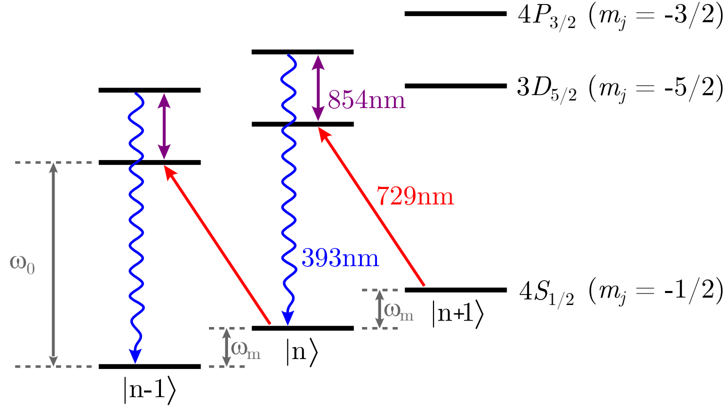

Figure 2.5: Sideband cooling process for a red detuned ($\delta = -\omega_{\mathrm{m}}$) qubit laser with 729 nm wavelength. The laser drives the transition $|S, n\rangle \rightarrow |D, n-1\rangle$, thereby reducing the motional quantum number by one phonon. The population is pumped to the $P_{3/2}$ state by using the 854 nm repumping laser, from where it rapidly decays to the ground state.

2.4.3 State initialization

The first step before quantum operations are performed on a trapped ion is to prepare the ion in the desired initial state, which is the $S_{1/2}(m_j = -1/2)$ state in this work. This process is also called *state initialization*. Two methods for state initialization are used for the ion traps presented in this thesis, either driving an electric dipole transition, or an electric quadrupole transition, both also referred to as optical pumping.

In order to populate the ground state using a dipole transition, a common technique is to use circularly polarized laser light of 397 nm wavelength, aligned along the quantization axis. Laser light with this polarization drives only the $S_{1/2}(m_j = 1/2) \rightarrow P_{1/2}(m_j = -1/2)$ transition. Occupation of the desired ground state $S_{1/2}(m_j = -1/2)$ is typically realized in less then 1 ms with high probability of > 0.99 [54] and thus gives a reliable technique for state initialization. Nevertheless, this process is limited by the polarization and alignment of the laser with respect to the quantization axis [45].

The second scheme to prepare the ion in the desired ground state is to address the optical pumping transition $S_{1/2}(m_j = 1/2) \rightarrow D_{5/2}(m_j = -3/2)$ [55]. The metastable $D_{5/2}$ state is coupled to the $P_{3/2}$ state by applying the 854 nm repumping laser, from

where it decays to the $S_{1/2}(m_j = -1/2)$ ground state. Additionally, the 866 nm repumping laser is used to increase the speed of the initialization process by repumping population from the $D_{3/2}$ to the ground state via the P state. Since this method is based on a quadrupole transition, the initialization process generally takes longer compared to the first described technique.

2.4.4 State detection

To detect the electronic state of an ion, we make use of the state-dependent fluorescence when illuminating the ion with the 397 nm cooling laser, driving the transition between the $S_{1/2}$ ground state and the $P_{1/2}$ state. Fluorescence photons are scattered and collected electronically with a charge-coupled device (CCD) camera or photomultiplier tube (PMT) (see section 4.4.3). If the ion is in the $S_{1/2}$ ground state, photons are emitted and the ion appears *bright*. If the ion is in the $D_{5/2}$ qubit state when illuminated with the laser, no photons are scattered, thus appearing *dark*. This technique is also called *electron shelving* [56].

Chapter 3

Scalable ion traps

There are several challenges to perform large-scale quantum information processing with trapped ions, with three major ones given by: i) scaling the ion trap to a large number of individually controllable qubits, ii) a constant gate performance when increasing the number of trapped ions, and iii) a high connectivity of single ions in the trap. Today, quantum registers with up to 150 ions have been trapped in a linear ion trap within one potential well [23]. However, there are challenges in scaling up to a large number of ions [33]. Individual addressing of single ions for manipulation and readout requires tightly focused laser beams. Due to a weaker coupling of the laser to the motion of the ions with an increased mass of the quantum bus, gate times increase and gate fidelities drop [57]. Moreover, with an increasing number of ions also the number of motional modes increases, causing spectral crowding. This prevents the spectral separation and thus individual motional frequencies of the ions cannot be addressed. In order to circumvent these issues in the scaling of ion traps, the following two approaches are pursued:

- modular ion traps: The ion string can be divided into smaller modules in order to mitigate the aforementioned drawbacks of long ion chains. Connecting these modules is either realized by directly shuttling the trapped ions in between different functional zones of the ion trap, also referred to as quantum charge-coupled device (QCCD) architecture [26], or by photonic interconnects used for remote entanglement between distant ion traps [58, 59]. Entangling ions trapped in separate potential wells in the QCCD architecture requires shuttling and reordering of ion strings. When using a two-dimensional geometry to form a network of entangled ions, the integration of junctions is necessary [26, 60]. However, during transport through junctions the ions gain kinetic energy, exciting the motional state [61]. One approach to address this problem is the implementation of sympathetic cooling with a second ion species to avoid destroying the stored information [62].

The approach of integrating photonic interconnects allows for entangling ions which are trapped in isolated traps or even in separate vacuum systems. Though, the collection of photons emitted by the ions is limited as the photons propagate in all directions of space, with the highest achieved collection efficiencies being in the range of $0.02 - 0.04$ [33]. Most likely, photonic interconnects will be needed for all architectures with more than 1000 ions.

- ion trap lattice arrays: Single ions are confined in individual trapping sites, enabling a two-dimensional lattice of trapped ions. Therefore, single ions are controlled individually in the trap. In order to perform quantum operations, the inter-ion distance needs to be small enough to achieve significant coupling via Coulomb interaction between neighboring ions [32]. Gate operations between two ions in adjacent potential wells have already been demonstrated [30, 31]. However, the speed achievable when moving quantum information in a 2D array is slow compared to a QCCD architecture [33].

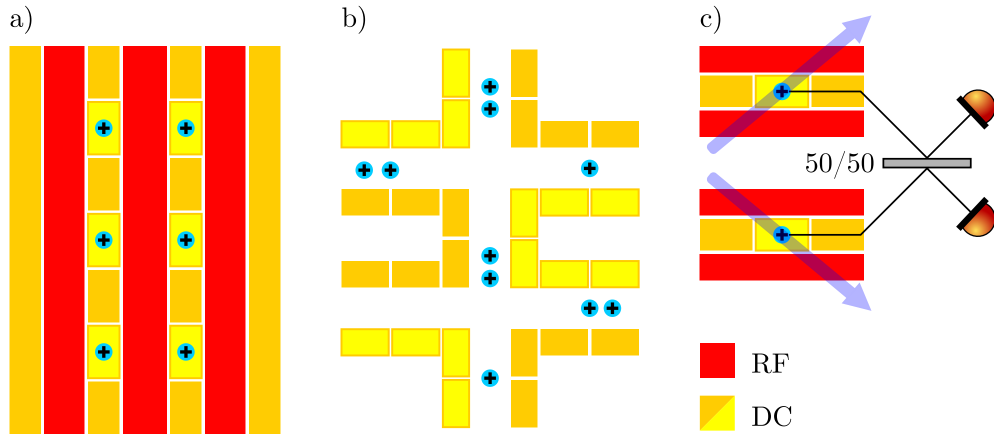

Figure 3.1: Approaches for the scaling of ion traps. a) Two-dimensional ion trap array. This architecture allows for individual trapping of single ions, forming a lattice array. b) QCCD architecture. The ion trap is divided into functional zones, between which the ions are shuttled. c) Photonic interconnects. In this modular approach, distant ions are connected via remote entanglement through emitted photons.

Both modular ion traps as well as ion trap lattice arrays require a segmentation of the trap electrodes, to generate a lattice of potential wells, referred to as a multi-well. In figure 3.1, all three scaling approaches are sketched. Segmented ion traps can be manufactured by microfabrication, allowing for complex trap layouts that support

scaling to large numbers of trapped ions. In this thesis, two microstructured ion trap architectures are discussed, one of them being a surface trap with electrodes in a single plane, and the other one consisting of two electrode layers to form a 3D architecture. This chapter focuses on the scaling of ion traps via microfabrication and the associated challenges related to motional heating due to a smaller ion-surface distance.

3.1 Microstructured ion traps

Early Paul traps used in ion trap experiments have been macroscopic traps with electrodes formed by rods [63]. Later, the rod electrodes have been exchanged by blades to allow for better optical excess [64, 65]. These traps facilitate a deep confinement potential and enable trapping of long ion strings. Nevertheless, to achieve a better control of single trapped ions, an increasing segmentation of the trap electrodes is necessary. Thus, the electrode size as well as the ion-electrode distance decreases to reduce distance to and time for shuttling operations. Thus, microstructured ion traps were developed, that can be manufactured precisely and enable the electrical connection of highly segmented electrodes. We distinguish between microstructured surface traps, in which the electrodes reside in only one plane, and three-dimensional traps, which make use of multiple layers to create the confining potential.

3.1.1 Surface traps

In a surface ion trap, all trap electrodes reside in a single plane, confining the ion in the generated electric field [66]. Two parallel RF rails alternate with GND/DC electrodes, creating the quadrupole potential, which confines the ion in the radial direction. A segmentation of the DC electrodes, as shown in figure 3.2, enables confinement along the trap axis (axial direction). Depending on the electrode segmentation, ions can be trapped either in a single potential or in a multi-well along the trap axis. In figure 3.3 a schematical cross section of a standard electrode geometry as well as the corresponding pseudopotential is depicted.

Initial attempts to make the ion trap smaller were based on laser-machined wafers made of insulating material that are subsequently coated with a single metal to generate electrodes [67]. Later, various surface traps have been fabricated and tested, with different substrate materials such as fused-quartz [68], fused silica [69], sapphire [70], or silicon [71, 72], using electrode materials such as gold, copper, aluminum, or highly-doped silicon. However, these traps were limited in complexity, because only a single metal layer was used to electrically connect all trap electrodes. In order to realize more complex trap layouts, recent traps were fabricated using complementary metal-oxide-

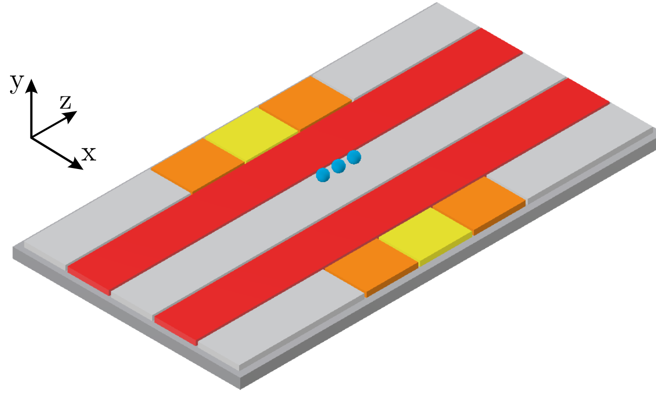

Figure 3.2: Schematic of a standard surface ion trap with RF (red) and segmented DC electrodes (gray, orange, yellow) with one potential well to trap multiple ions (blue circles).

semiconductor (CMOS) compatible technologies [73]. In this way, multiple functional metal layers can be used for electric leads. Moreover, this opens the possibility to include functionality such as integrated electronics [36, 37] or through-substrate vias (TSVs) [35], for connecting electrodes to an underlying carrier board and thus minimizing the trap size.

Surface traps facilitate optical access laterally as well as from top. Lasers are

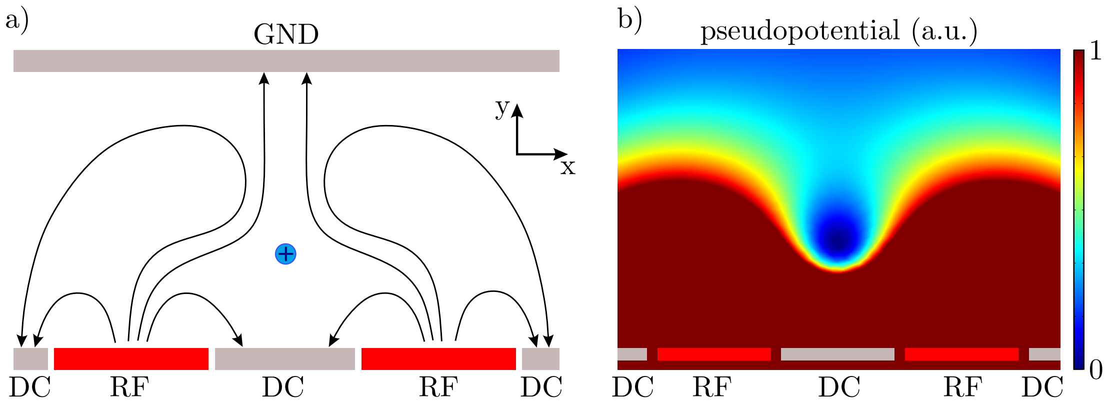

Figure 3.3: Surface ion trap with RF (red) and DC (gray) electrodes. a) Schematic cross section of the electrode geometry in a standard surface trap. The ion (blue circle) is confined in the stray field of the RF (red) and DC (gray) electrodes, generated by the electric field lines (black lines). b) Simulated pseudopotential in a surface ion trap with a minimum (blue) above the trap center, in which the ion is trapped.

generally aligned in parallel to the trap surface to avoid stray light reflected from the chip surface. However, this limits the NA of the lateral optical access dependent on the ion-surface distance. As the laser has no propagation component in the vertical direction (see section 2.4), a tilt of the ion's motional mode axis is necessary to enable laser cooling in all three directions. A tilt of the mode axis can be realized by an asymmetric electrode geometry, where the RF electrodes have different widths [74], or by applying an appropriate voltage set to the segmented DC electrodes to rotate the potential [69]. If the size of the ion trap increases, clipping of the laser light on the chip edges can lead to increased stray light. Thus, integrating a vertical slit through the trap chip allows for laser access perpendicular to the trap surface [75, 76], which reduces stray light and laser-induced charging of the trap chip. Moreover, such a slit could also be used for ion loading.

Due to the rather weak confinement potential of surface traps of typically a few tens to hundreds of electronvolts, the lifetime of the ions in the trap is reduced, as the probability of ion loss due to collisions with background gas molecules is increased compared to three-dimensional traps. Therefore, an ultra-high vacuum environment is needed. Operating the trap at cryogenic temperatures of a few Kelvin reduces both the amount of background gas due to a higher vacuum, as well as the inherent kinetic energy of remaining particles [77, 78].

Surface trap arrays

A precise microfabrication of ion traps allows for segmenting the trap electrodes to thousands and more electrodes arranged in a complex geometry. Therefore, scalable designs such as the QCCD architecture or 2D lattice arrays can be realized. In this thesis, a surface trap forming a two-dimensional ion trap array is presented (see section 4). One approach to create a 2D lattice of trapped ions is to use multiple RF rails alternated with segmented DC electrodes, thus creating parallel linear traps, as depicted in figure 3.4. Here, the axial multi-well is provided by segmented DC electrodes. Because the RF electrodes are formed by parallel rails, multiple ions can be trapped in one trapping site along the trap axis [79].

To perform quantum operations on the trapped ions, one requirement is entanglement of the ions. While ions in a single potential well are coupled via their shared motion, motional coupling of ions in separate potential wells can be achieved by the Coulomb interaction. Such a link via the Coulomb interaction requires small inter-ion distances s of a few tens of micrometers [80]. The coupling strength Ω_c through Coulomb interaction between two ions in separate potential wells is given by

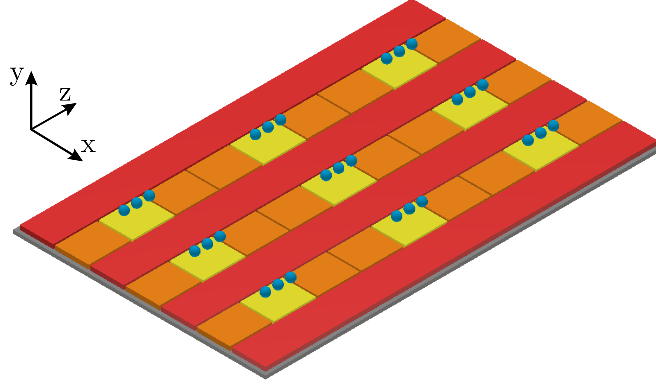

Figure 3.4: Schematic of a 2D ion trap lattice array with alternating RF (red) and segmented DC electrodes (orange, yellow) to create a confining multi-well for trapping ions (blue circles) in two dimensions.

$$\Omega_{\mathrm{c}} = \frac{Q^2}{2\pi\varepsilon_0 M}\frac{\varsigma_j}{\omega_m s_j^3} \tag{3.1}$$

with the motional frequency ω_m of the ions [31]. Here, $\varsigma_j = 1$ for the coupling direction $j = z$ along the axial multi-well, and $\varsigma_j = 1/2$ for the coupling direction $j = x$ in radial direction across the multi-well defined by the RF electrodes. The spacing between the ions in z-direction (x-direction) is denoted s_z (s_x). Equation (3.1) indicates a strong dependence of the coupling strength on the inter-ion distance, therefore a small distance between neighboring trapping sites is desirable. The potential generated by the trap electrodes decreases exponentially with an increasing ion-surface distance [81]. This limits the ion-surface distance dependent on the electrode dimensions, with a suitable potential multi-well requiring an ion-surface distance d smaller than the lattice constant s ($d \lesssim s$). Electrodes with the size of only a few micrometers can be precisely manufactured by microfabrication techniques, enabling a small inter-ion distance at a low ion-surface distance. However, motional heating of the ions significantly increases with a decreasing ion-surface distance [82]. Hence, a sufficiently large ion-surface distance (usually a few tens to hundreds of micrometers) is necessary to achieve high-fidelity qubit gates. To be able to meet both requirements of high-reliability gates as well as a small inter-ion distance for the exchange of quantum information, shuttling of the ions inside the trap array is needed to reduce the inter-ion distance for appropriate coupling strengths while keeping heating rates low. A description of ion shuttling in the 2D array is given in section 4.1. A scheme how to entangle ions in a 2D ion lattice array is given in [79].

3.1.2 Three-dimensional ion traps

In contrast to surface traps, multiple layers of electrodes are used to confine ions in 3D ion traps. A schematic of a two-layer ion trap is depicted in figure 3.5. A simple two-layer ion trap consists of two pairs of RF and DC electrodes, which are arranged diagonally to each other in order to generate a point symmetrical confining potential in radial direction. A segmentation of the DC electrodes provides confinement along the trap axis. Implementing a further segmentation of the DC electrodes allows for multiple individual trapping sites and enables ion shuttling along the trap axis. A schematic of a 3D ion trap cross section and the corresponding pseudopotential is shown in figure 3.6.

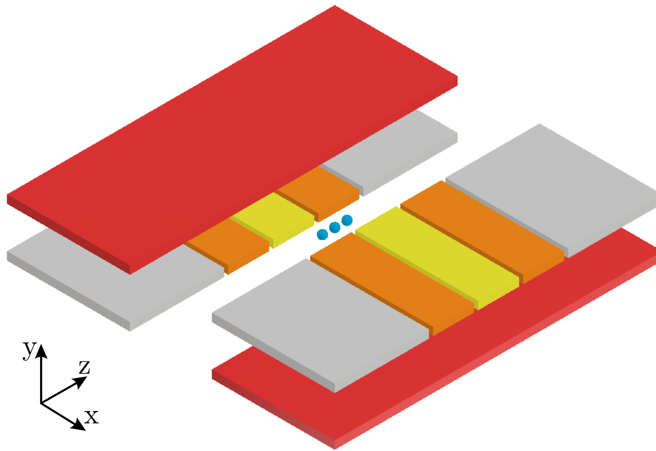

Figure 3.5: Schematic of a segmented two-layer ion trap. A segmentation of the DC electrodes (gray, orange, yellow) creates a confining potential in axial direction (z-direction). In combination with the RF electrodes (red) the ions (blue) are confined in all three dimensions.

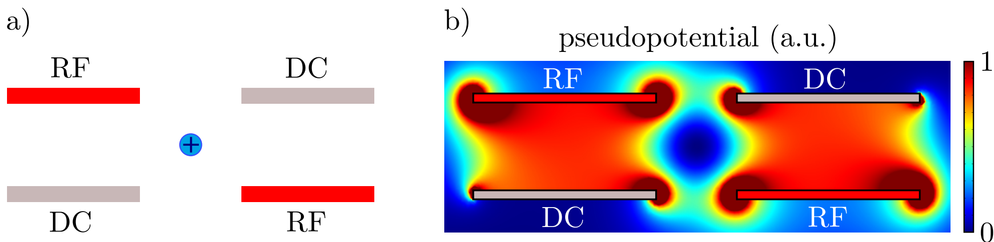

Figure 3.6: Two-layer ion trap. a) Electrode geometry with two pairs of RF (red) and DC (gray) electrodes arranged to trap an ion (blue circle) in the trap center. b) Pseudopotential of the two-layer ion trap with a potential minimum (blue) in the trap center.

Arranging the electrodes in a 3D architecture with diagonally configured RF and GND electrodes leads to a notably deeper trap depth in multilayer-traps of 1 eV and higher compared to surface traps with trap depths in the range of a few tens to hundreds of electronvolts [23, 33]. Due to the associated higher confinement, 3D traps are less susceptible to ion loss caused by collisions with background gas molecules. Moreover, these traps show a higher curvature at the ion's position, that needs to be compensated for in surface traps.

To achieve a high level of segmentation of the trap electrodes combined with a smaller trap size, laser-machined ion trap devices based on metal-coated alumina have been developed [67, 83]. In such traps, several wafers are stacked and connected by either glueing or clamping to generate a 3D trap architecture. A different approach uses electrodes patterned on the front and back side of a silicon wafer, thus creating a three-dimensional trap structure, given by the thickness of the silicon substrate of 340 µm [84]. The silicon substrate as well as additional layers of silica, which support the gold electrodes, are etched to form the aperture for ion trapping in the center between the electrodes. Ion shuttling [19, 83, 85, 86] as well as ion transport through junctions [61, 87] have been demonstrated in stacked alumina traps. Recently, laser-machined fused-silica wafers were investigated as ion trap substrates [21, 88], as these can be fabricated with a precision up to $1 - 2$ µm and allow for more complex trap layouts.

Moreover, commercial semiconductor microfabrication techniques such as micro-electro-mechanical systems (MEMS) technology can be used to fabricate multilayer ion traps. MEMS technology is attractive due to its compatibility with dielectric substrates such as fused silica or sapphire, as well as the possibility to realize 3D structures by electrodes on multiple wafers bonded to each other [89]. Furthermore, the technology allows the processing of wafers with through-substrate vias (TSVs) and holes (e.g. loading or detection slits). One approach using MEMS technology [90] to form a monolithic, three-dimensional ion trap is based on alternating layers made of GaAs and AlGaAs on a GaAs substrate. By etching, a through-hole as well as cantilever electrodes are generated, forming a 3D architecture. The use of commercial MEMS processes is advantageous because, next to a 3D architecture, also additional functionality such as photonics (e.g. waveguides) or electronics can be integrated, which is important for the further scaling of the ion trap.

3.2 Motional heating

An important condition for the execution of reliable quantum gates with ions is motional coherence. Electric field noise can lead to the excitation of secular modes, resulting

in an increase of the motional quantum number n. The motional heating rate Γ_h is defined by the change of the mean motional quantum number $\overline{n}$ with time

$$\Gamma_\mathrm{h} = \dot{\overline{n}} \tag{3.2}$$

or, in other words, how fast an ion in the trap heats up when it is not laser cooled. Heating of the ions leads to decoherence and can shift the ion out of the Lamb-Dicke regime, thus reducing the number of gates that can reliably be performed sequentially on the ions without the need of cooling. Moreover, the fidelity of entangling gates reduces due to motional decoherence [91]: a heating of motional modes during gates increases the chance of errors.

3.2.1 Sources of heating

Electric field noise at the ion's position results in an increasing temperature of the ion. With the electric field noise spectral density S_E, the heating rate of the ion is then given by [92]

$$\Gamma_\mathrm{h} = \frac{Q^2}{4M\hbar\omega_m} S_E, \tag{3.3}$$

where Q and M are the ion's charge and mass, ω_m its motional frequency, and $\hbar$ the reduced Planck constant. There are various sources for electric field noise, such as technical noise caused by the drive electronics, Johnson-Nyquist noise [93, 94], and surface noise [92]. Technical noise is usually related to the DC and RF voltage supply and is not dependent on the trap temperature. Electrical filters in the supply lines of the trap electrodes are a common method to reduce technical noise. In the following, we briefly discuss the most important sources of electric field noise in ion traps and present different concepts for noise mitigation.

Note, that the electric field noise present in ion traps is not fully understood yet [92]. Therefore, the heating caused by electric field noise is also known as *anomalous heating*.

Johnson-Nyquist noise

The motion of charge carriers in the trap electrodes due to thermal fluctuations causes electric noise, known as Johnson-Nyquist noise (JN) [93, 94]. At a resistor with resistance R, the spectral density of voltage noise is given by

$$S_V = 4k_\mathrm{B}TR \tag{3.4}$$

with k_B the Boltzmann's constant and the temperature T of the resistor. This voltage noise relates to electric field noise at the ion's position

$$S_E = \frac{S_V}{\delta_c^2} \tag{3.5}$$

with δ_c the characteristic distance. This parameter is dependent on the trap geometry and translates the voltage noise of an electrode to the corresponding electric field noise at the ion's position [92]. The model for estimating JN relies on an ideal resistor generating white noise. JN is especially important in highly-segmented, microstructured ion traps, where small electrical leads with corresponding resistance are needed for contacting all trap electrodes [29]. In most cases, the resistance of the electrical leads is higher than that of the electrodes themselves.

Surface noise

Another source of noise for ion traps is *surface noise*, which is caused primarily by effects on the trap surface. A common explanation of surface noise is based on so-called patch potentials, which are found on non-homogeneous electrode surfaces, that arise due to different crystal orientations, grain structures or adsorbates on the surface [92]. Example models are two-level fluctuators (TLFs), where electrons or atoms collect in local minima, or adatom diffusion, in which adsorbed atoms diffuse on the trap surface, resulting in a changing dipole distribution with time [92].

Surface noise is strongly dependent on the ion-surface distance, with a scaling of around $S_E \propto d^{-4}$ [95, 96] dependent on the geometry. In some cases, the noise was found to increase with rising temperature [97, 98], thus trap operation at cryogenic temperatures helps to reduce electric field noise induced by the trap surface.

Noise mitigation

There are several methods to reduce motional heating of the ions and thus preventing motional decoherence. One technique is to use low-noise electronics and integrate low-pass filters for the DC supply lines in order to decrease technical noise generated by the electrodes. The electric filters should be placed as close as possible to the ion trap to reduce the unfiltered lead length, and the filter design should not produce JN due to additional resistors. To reduce JN, the resistance of the leads connecting the trap electrodes to the bonding pads used for wirebonding should be as low as possible, thus conducting materials with a low resistivity (e.g. copper) are recommended. The question of the perfect material for reduced surface noise in ion traps is still open, while requirements like a high conductivity and low power dissipation are clearly defined [99]. However, implementing an in-situ surface cleaning of the trap electrodes by ion bombardment with argon ions proved to be useful in reducing the heating rate up to a

factor of 100 [100]. Moreover, operating the ion trap at cryogenic temperatures helps decreasing motional heating due to thermally activated surface noise sources by about two orders of magnitude [92].

3.2.2 Measuring the heating rate

There are different methods to determine the heating rate of an ion trap. In this section, we look at two techniques performed on the ion traps presented in this thesis. Both of these methods are based on Rabi oscillations of the motional sidebands of the quadrupole transition. First, the ion is laser cooled by Doppler cooling followed by resolved sideband cooling. After a certain waiting time, a laser pulse with the 729 nm qubit laser drives Rabi flops on the red or blue sideband. The occupation probability of the sideband is then used to gain information about the motional state. As the last step, the ion's electronic state is detected with the ion shelving method as described in section 2.4.4.

Rabi oscillations

If the heating rate of an ion trap is in the moderate regime with a quantum number $\overline{n} = 5 - 20$, investigating the Rabi oscillations on a sideband for the $S_{1/2} \to D_{5/2}$ transition can be used to determine the heating rate. The first order Rabi frequencies for the red and blue sideband in the Lamb-Dicke regime are defined as [44]

$$\Omega_{\text{red}} = \Omega_{n,n-1} = \Omega_0 \eta \sqrt{n} \tag{3.6}$$

$$\Omega_{\text{blue}} = \Omega_{n,n+1} = \Omega_0 \eta \sqrt{n+1} \tag{3.7}$$

with the Lamb-Dicke parameter η and the carrier Rabi oscillation frequency Ω_0. The excitation probabilities for red and blue sideband transitions are given by

$$P_D^{\text{RSB}} = \frac{1}{2} + \left(1 - \sum_{n=0}^{\infty} P_n \cos\left(\Omega_{n,n-1} t\right)\right) \tag{3.8}$$

$$P_D^{\text{BSB}} = \frac{1}{2} + \left(1 - \sum_{n=0}^{\infty} P_n \cos\left(\Omega_{n,n+1} t\right)\right), \tag{3.9}$$

where P_n is the occupation probability for the motional state n. $\Omega_{n,n\pm1}$ are the coupling rates defined in equations (3.6) and (3.7), and t is the pulse length of the laser. Here, the distribution is assumed to be thermal

$$P_n = P_{th} = \frac{\overline{n}^n}{(1+\overline{n})^{n+1}}. \tag{3.10}$$

By fitting the excitation probability from equation (3.8) or (3.9) to the measured Rabi oscillation data, the mean phonon number and thus the heating rate can be extracted.

Sideband ratio method

If the motional quantum number is small ($\overline{n} \leq 1$), a similar method based on the sideband Rabi oscillations can be used, also referred to as the *sideband ratio method*. The ratio between the excitation probabilities for the red and the blue sidebands prepared in identical motional states is given by

$$\overline{n} = \frac{R}{1-R} \tag{3.11}$$

for the assumption of a thermal distribution of the state and with

$$R = \frac{P_D^{\mathrm{RSB}}}{P_D^{\mathrm{BSB}}}. \tag{3.12}$$

Since this method is independent of the Rabi frequency, the Lamb-Dicke parameter and the pulse length, the mean quantum number for different wait times can be determined, enabling the calculation of the heating rate.

Chapter 4

2D linear ion trap array

The contents of this chapter have been published in the article "2D Linear Trap Array for Quantum Information Processing", P. Holz et al., Advanced Quantum Technologies (2020) [29].

The 2D ion trap array was designed by Philip Holz and Gerald Stocker. Fabrication and electrical characterizations were carried out at Infineon Technologies by the author. Investigations on the trap performance in the experiment were conducted by the author and Marco Valentini.

Ion trap lattice arrays exhibit two main advantages: i) ions trapped in a single trapping site do not show excessive micromotion compared to a 2D ion string consisting of multiple ions formed in a single potential well in linear traps [101], and ii) a precise control of the confinement potential is provided, therefore enabling the realization of different array structures, such as a rectangular or triangular lattice, depending on the geometry and control voltages [29]. A segmentation of the trap electrodes provides multiple trapping sites structured in an array, forming a so called potential multi-well. However, confining a large number of ions in a potential multi-well requires complex trap layouts with a large number of individually controllable trap electrodes, which can only be realized by microfabrication.

This chapter concentrates on the microfabrication and characterization of a two-dimensional linear ion trap array designed to perform quantum information processing based on ions trapped in two parallel linear arrays. First, the trap design and layout is discussed, followed by a detailed description of the microfabrication conducted at the cleanroom facilities of Infineon Technologies Austria in Villach. Then, an overview of the electrical characterization of the trap chips is given. In the last section experimental

results with respect to the ion trap performance are presented.

4.1 Concept

The goal of a 2D ion trap array is a well-connected lattice of qubits to facilitate gate operations on a large scale. Such a lattice array can be realized by microstructured ion traps that are highly segmented, so that every single ion is trapped in an individual trapping potential. A first approach to form a 2D ion trap lattice in this research group was based on multiple point traps, arranged in an array [102]. This method has the disadvantage of requiring multiple RF sources to provide independent RF voltages for every single point trap in the array. A different approach is given by linear arrays of ions, arranged in parallel to form a two-dimensional lattice. Here, the 1D ion trap array is confined in z-direction using segmented DC electrodes, thus forming a multi-well along the trap axis.

To enable gate operations between ions in different trapping sites of such a 2D trap array, motional coupling of the ions is required. The motional coupling rate Ω_c between two ions through Coulomb interaction as defined in equation (3.1) is strongly dependent on the inter-ion distance s_j with $\Omega_c \propto s_j^{-3}$ [31]. Thus, to entangle two ions in the lattice array, a maximum distance of a few tens of micrometers between the ions is required to achieve a coupling strength in the range of kHz, which allows for coherent operations [29–31]. The spacing between two neighboring ions is given by the width of the trap electrodes providing the trapping potential. Between the linear arrays this is defined as $s_x = w_{RF} + w_{DC}$, with the width of the RF electrode w_{RF} and the segmented DC electrodes w_{DC}, respectively. Aiming for an inter-ion distance of around 40 µm to enable coherent operations, a maximum ion-surface distance of $d \approx 30\,\mu\text{m}$ can be achieved [29]. However, since the anomalous heating of trapped ions increases with d^{-4} with the ion-surface distance 3.2.1, sufficiently large ion-surface spacings are desirable [103]. In this case, neighboring ions need to be moved in the trap by applying suitable voltage sets to DC and RF electrodes to reduce their distance and therefore enable motional coupling, while maintaining a suitable ion-surface distance.

Shuttling of the ions in the array is achieved by suitable tuning of RF and DC voltages, as described in figure 4.1. The inter-ion spacing in axial direction is tuned by applying appropriate voltages to the segmented DC electrodes. With this method, either the whole 1D ion array is moved in the same direction, or the inter-ion distance is reduced to enhance coupling in axial direction. Coupling between ions in two parallel linear ion traps is achieved by decreasing the voltage amplitude of the RF electrode in between the ion strings. This leads to a shift of the potential minimum for both

trapping sites, reducing their distance, as visualized in figure 4.2. If multiple 1D ion arrays are placed in parallel, only two alternating, independent RF voltages are needed to achieve coupling of the ions between the 1D ion arrays in the whole lattice. Using a tunable RF electrode is advantageous to reduce anomalous heating, since it enables a significantly increased ion-surface separation compared to ion traps with fixed RF voltage.

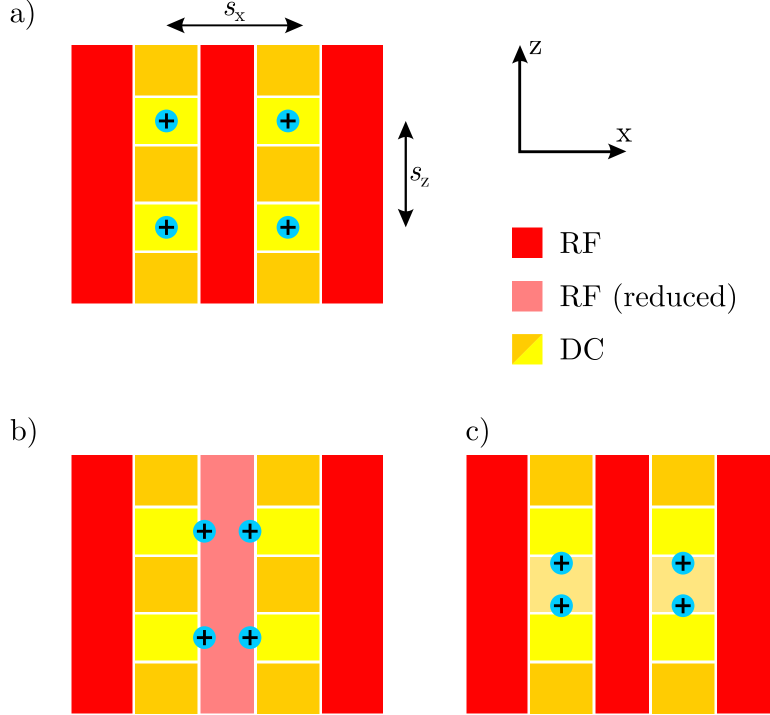

Figure 4.1: Schematic illustration of next-neighbor coupling in a 2D ion lattice array. a) Ions (blue circles) are trapped in a two-dimensional multi-well created by RF (red) and DC (shades of yellow) electrodes with inter-ion distance s_x in radial (x) and s_z in axial (z) direction. b) By reducing the voltage of the central RF electrode (light red) the distance of ions in adjacent trapping sites in radial direction decreases, enabling coupling of the ions via Coulomb interaction. c) By changing the voltages of the segmented DC electrodes, the inter-ion distance is tuned to achieve coupling along the axial direction.

Ion shuttling in the trap allows not only for coupling neighboring ions, but also supports different lattice connectivities like a rectangular and triangular configuration, see figure 4.3. Furthermore, by shuttling ions along the array followed by an entangling operation in the perpendicular lattice direction, coupling between next-nearest ions or ones that are even further apart can be achieved. This allows for complicated lattice

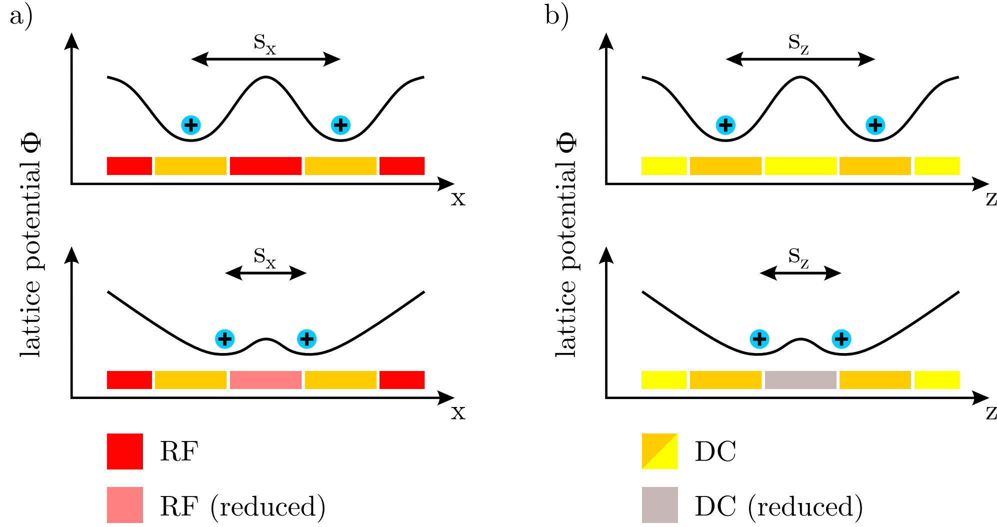

Figure 4.2: Schematic illustration of shuttling ions in a 2D ion lattice array by changing the voltages of RF (red) and DC (shades of yellow) electrodes to manipulate the lattice potential. a) Ions (blue circles) are shuttled along the radial direction (x) of the array by reducing the RF voltage of the central RF electrode (light red). b) By reducing the voltage of a DC electrode (gray) between two trapped ions, the inter-ion distance is tuned to achieve coupling along the axial direction (z).

connectivities and moreover for the transport of quantum information through the lattice [29].

A design for a prototype 2D ion trap array was developed by Philip Holz and Gerald Stocker at the University of Innsbruck. This ion trap provides two parallel 1D ion strings confined in a microfabricated ion trap and is referred to as the 2D twin trap. It represents a minimum instance design of two ion strings forming a 2D lattice array. An extension of the layout in both directions enables a larger lattice with more than 100 trapped ions used as qubits for quantum information processing and quantum simulations [79]. This section reviews the trap geometry, and describes the used layer stack and design rules for the fabrication process.

4.1.1 Trap geometry

The concept of the 2D twin trap is based on forming a potential multi-well in two directions, using segmented DC electrodes along the trap axis and in total three RF electrodes. A detailed simulation of the geometry and operating parameters of the ion trap is given in Philip Holz's PhD thesis [79] and Gerald Stocker's master thesis [104].

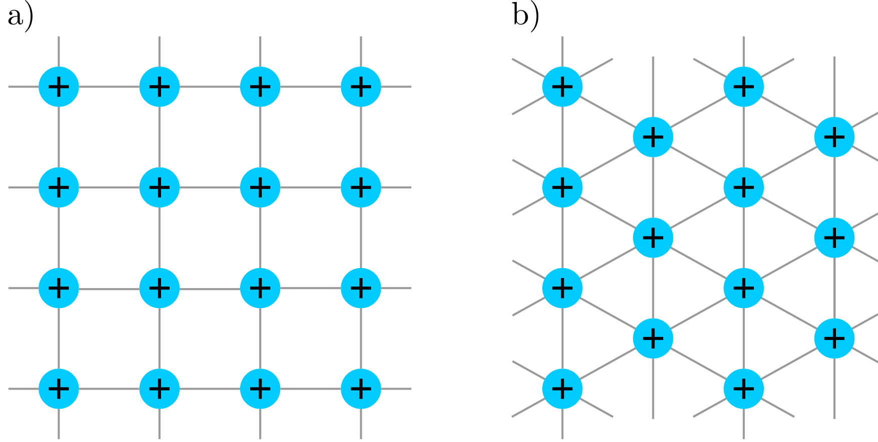

Figure 4.3: Illustration of a a) rectangular and b) triangular two-dimensional lattice of ions (blue circles) with corresponding next-neighbor interactions (connecting gray lines).

Two designs of the 2D twin trap are developed, aiming for an ion-surface distance of 80 µm and 120 µm. The dimensions of several electrodes for the 120 µm design are listed in table 4.1. The inner RF rail has a width of 64 µm, both outer RF rails are 243 µm wide. The segmented DC electrodes have a dimension of 93 µm × 93 µm. These electrodes are also referred to as "island" electrodes as they need to be routed in a lower metal layer due to a lack of space in the top metal layer. In the trap center, the innermost DC island electrode is further split into three equally-sized parts adding up to a normal-sized DC segment to reduce the inter-ion distance between ions in z-direction. Next to the outer RF electrodes additional DC electrodes are placed as these are needed for micromotion compensation. These compensation electrodes have a width of 193 µm. Gaps between trap electrodes are 9 µm.

Table 4.1: Electrode dimensions of the 2D twin trap in radial direction (x)and along the trap axis (z).

electrode	width along x (µm)	length along z (µm)
RF_{out}	243	6000
RF_{center}	64	6000
DC_{island}	93	93
$DC_{interaction}$	93	25
$DC_{com,out}$	193	2842
$DC_{com,center}$	193	297

This electrode geometry enables two different configurations of operation, dependent on the connectivity of the segmented DC electrodes. In the first configuration, the segmented DC electrodes forming the potential multi-well along the trap axis are periodically connected so that every third electrode shares the same voltage. This allows for shuttling the whole ion chain along the trap axis, see figure 4.4a. In the second configuration, the interaction zone in the trap center is used to reduce the inter-ion distance of two ions trapped in the innermost trapping sites along the trap axis. Here, the central DC electrode is further split into three independent electrodes, as shown in figure 4.4b.

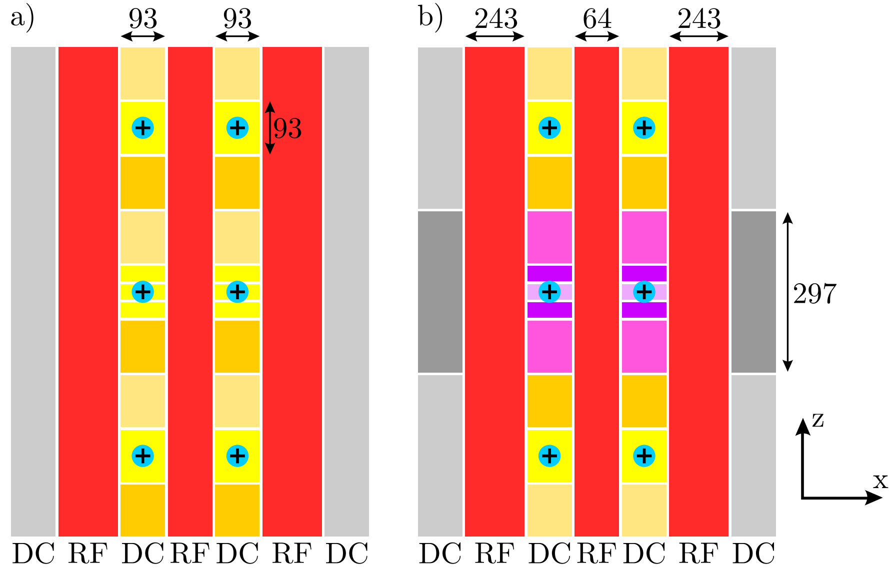

Figure 4.4: Schematic geometry of the 2D twin trap with two operation configurations. a) The segmented DC electrodes forming the potential multi-well along the trap axis (shades of yellow) are periodically connected so that every third electrode shares the same voltage. Thus, above every third electrode an ion (blue circle) is confined. b) The interaction zone in the trap center is used to reduce the inter-ion distance of the two ions trapped in the innermost trapping sites. Here, the central DC electrode is split into three independent electrodes (shades of purple). Electrode sizes are noted in micrometer units.

4.1.2 Routing and layer stack

Due to the large number of trap electrodes, multiple metal layers are necessary for routing the electrical leads from the island electrodes to the bond pads located at the edge of the trap chip. In total, six functional layers are forming the ion trap, divided

in three conductive metal layers and three dielectric layers. These dielectric layers are also referred to as inter-metal oxide (imox) layers as they are deposited between the metal layers for electric isolation. In table 4.2 all layers with corresponding materials and layer thickness are listed and are visualized in figure 4.5.

Table 4.2: Layer stack of the ion traps with material, target thickness and measured thickness.

layer	material	thickness (nm)	thickness measured (nm)
metal 3	AlSiCu	2000	2140
imox 2	SiO_x (deposited)	2200	2150
metal 2	AlSiCu + TiN	1000 + 25	1020
imox 1	SiO_x (deposited)	2200	2170
metal 1	AlSiCu + TiN	750 + 25	784
bottom oxide	SiO_2 (thermal)	1300	1310
substrate	Si	725000	725000

Figure 4.5: Schematic layer stack of the ion trap wafers on the silicon substrate (dark gray). Metals are colored gray, oxide blue.

The metal layers are made of AlSiCu, an alloy mainly consisting of aluminum. The addition of 1 % silicon avoids eutectic mixing with the silicon substrate [105]. Additionally, 0.5 % copper is included to increase the resilience to high currents. The metal leads and electrodes need to be low-Ohmic to minimize i) the RF pick-up voltage on adjacent DC electrodes and routing [106], ii) Johnson noise [93], and iii) heating of the 2 µm thin RF rails by capacitive loading currents. On top of the first two AlSiCu metal layers, a 25 nm thick titanium nitride (TiN) layer is deposited that improves the

adhesion of the deposited oxide on the AlSiCu layer and further acts as an anti-reflection coating for the light exposure during lithography of the oxide layers. The six functional layers are given by:

- **bottom oxide**: silicon dioxide created through thermal oxidation of the silicon substrate forming a 1.3 µm thick insulation layer between the first metal layer (metal 1) and the substrate. Thermal oxide has a low defect density and a low roughness of the interface.
- **metal 1**: AlSiCu deposited on the thermal oxide, with a thickness of 0.75 µm. This layer serves as a shielding layer: first, the substrate is shielded from the RF field to avoid heat loss due to RF pick-up in the substrate, and from laser light which could induce stray charges. Second, the ion is shielded from possible charge fluctuations in the substrate which cause a displacement of the ion from the RF null position and therefore increase micromotion and ion heating.
- **imox 1**: 2.2 µm thick silicon oxide (SiO_x with $x \approx 2$) deposited through low-temperature plasma deposition (wafer substrate is heated to 430 °C) on the metal 1 layer forming the electrical separation between metal 1 and metal 2.
- **metal 2**: AlSiCu deposited on the imox 1 layer, with a thickness of 1 µm. In this layer the electrical routing from the DC electrodes to the bond pads on the axial sides of the ion trap chip is realized. Connections to the metal layers above and below are created by vertical interconnect accesss (vias).
- **imox 2**: 2.2 µm thick silicon oxide (SiO_x) forming the electrical separation between metal 2 and metal 3 layer.
- **metal 3**: AlSiCu deposited on the imox 2 layer, with a thickness of 2 µm. This layer forms the DC and RF electrodes providing the electric fields creating the confinement potential.

In the complex trap layout, in total 80 electrodes need to be connected to the bond pads at the chip edge. The trap layout and routing is shown in figure 4.6. Electric connections (leads) are always routed in the thickest metal layer available to minimize their resistance. Due to a lack of space, the leads of the DC island electrodes are routed directly below the electrodes in the metal 2 layer. Here, the resistance is further halved by using two vias per electrode as connection between the metal 2 and metal 3 layer. In addition, this provides reliability through redundancy. To minimize parasitic capacitive coupling of the neighboring RF electrodes to the DC leads, additional GND lines are

included as shields beside the leads to reduce RF pickup on the DC electrodes. In general, RF pickup on DC electrodes should be avoided as it generates an electric field at the ion's position and thus induces micromotion and heating of the ions. For the same reason, DC leads are not routed directly below the RF electrodes, except in the interaction zone, where the leads to the segmented DC island electrodes need to cross the outer RF electrodes. The parasitic capacitance can be reduced by moving the leads to the metal 1 layer and defining a GND shield in the metal 2 layer in the crossing area. This minimizes RF pickup and shields the substrate. A detailed description of the routing is given in Gerald Stocker's master thesis [104].

The trap layout requires only three independent metal layers, but with growing complexity up to six metal layers can be realized with the chosen fabrication technology at Infineon. The current layer stack can still be structured well with optical lithography, but a higher topology can lead to insufficient edge coverage with photoresist. Thus, when using additional metal layers, a planarization of the surface is recommended, e.g. by chemical-mechanical polishing (CMP) [105] of the imox layers.

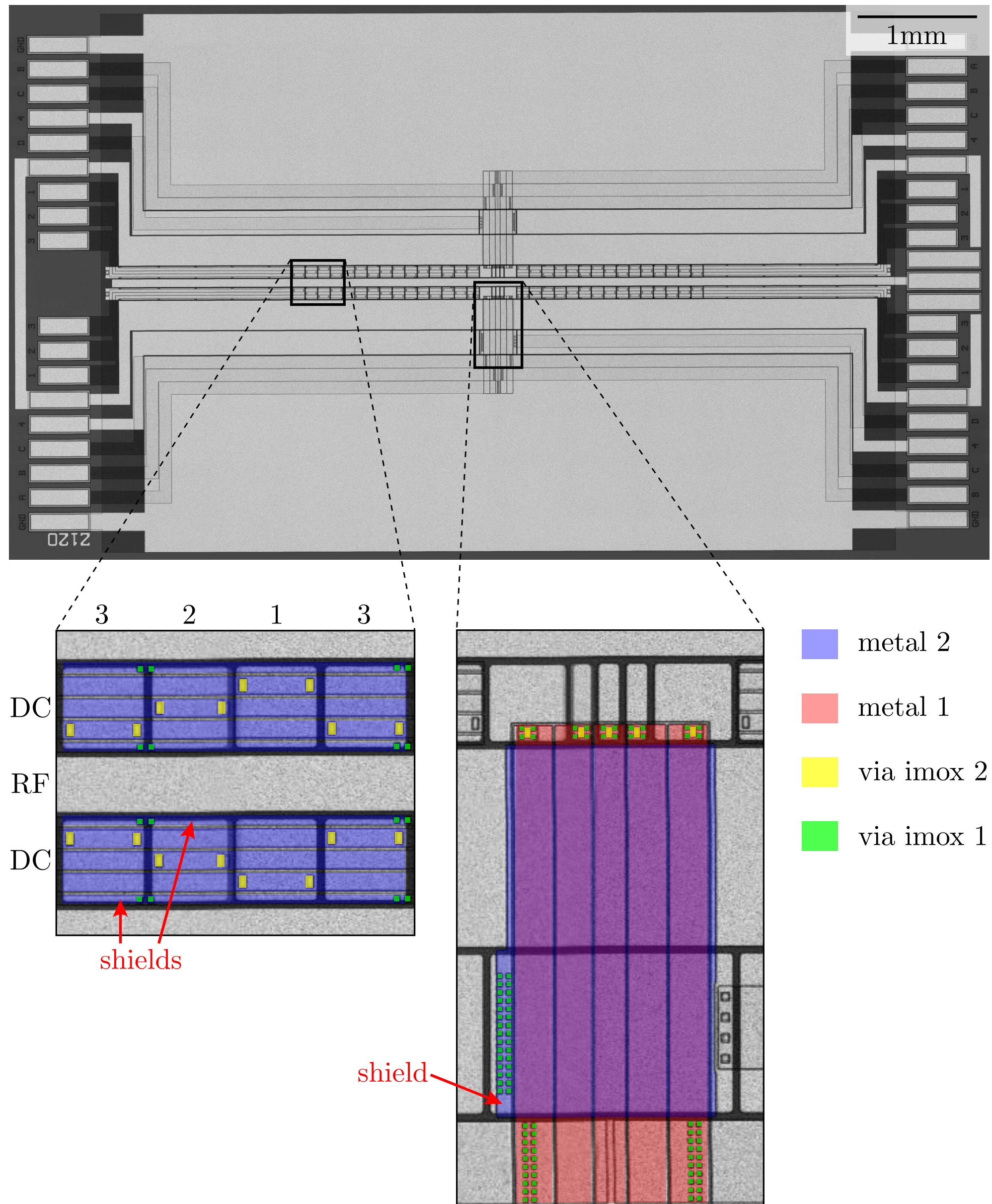

Figure 4.6: Microscopic image of the ion trap. Wire bond pads are located on two sides of the chip. The periodically connected DC island electrodes that form the confining multi-well in axial direction are routed with leads in the metal 2 layer (blue). To reduce parasitic capacitance of the RF electrodes to the DC leads, additional GND shield lines are placed next to the DC leads. In the interaction zone in the trap center, the leads to the further segmented DC island electrodes need to cross the outer RF electrodes. Therefore, the routing is moved to the metal 1 layer (red) and a GND shield is added in the metal 2 layer in the crossing area.

4.1.3 Design rules

Microfabrication in an industrial facility gives access to a wide tool park of fabrication processes and provides high precision in small geometry structures, if design rules regarding fabrication are adhered to. The design rules of a technology define the allowed dimensions for each available layer, depending on layer thickness, material and the used technique for structuring. The standard procedure for layer structuring consists of material deposition, optical lithography to produce the desired pattern, followed by an etching step. Design rules primarily concern the structure and gap widths that can be reliably resolved and etched. In table 4.3 the design rules for minimum gap and structure size of all three metal layers and the two imox layers are given. As an example, these design rules are visualized in figure 4.7 for the first metal layer.

Table 4.3: Design rules for minimum structure and gap sizes for the three metal layers and the two imox layers of the 2D twin trap.

layer	AlSiCu / TiN	etch process	minimum structure size	minimum gap size
metal 1	750/25 nm	plasma	2 µm	5 µm
imox 1	2200 nm	plasma	2.4 µm	2.4 µm
metal 2	1000/25 nm	plasma	2.8 µm	5 µm
imox 2	2200 nm	plasma	6 µm	12 µm
metal 3	2000 nm	wet	14 µm	9 µm

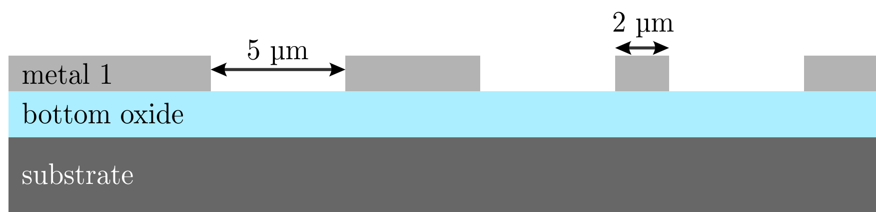

Figure 4.7: Design rules for the first metal layer (metal 1, gray), which is deposited above the bottom oxide (blue) on the silicon substrate (dark gray). The minimum gap size and minimum structure size are defined as 5 µm and 2 µm, respectively.

All layers except the metal 3 layer are etched with an anisotropic plasma etch, which removes material only in a direction perpendicular to the surface. This etching technique allows for having smaller gap and structure sizes compared to an isotropic wet etch, in which the material is etched in all spatial directions. Because the routing

of electric leads from the DC electrodes to the bonding pads is integrated in the metal 1 and metal 2 layer, small gap sizes are desired to enable broader leads to reduce their resistance. The minimum gap size in the metal 1 and metal 2 layers is mainly dependent on the thickness of the following 2.2 µm thick oxide layers. It must be assured, that the deposited oxide fills up the entire gap in the metal layer, without creating air pockets. Such air pockets could cause electrical failures [104]. Therefore, the minimum gap size is defined to be 5 µm for the metal 1 and metal 2 layer, and is achievable with anisotropic plasma etching. Due to the larger layer thickness of the metal 3 layer of 2 µm, we use an isotropic wet etch for structuring, which is already available at Infineon. Here, the masking layer is subjected to an under etch of the size of the etched layer thickness, increasing the etched area compared to the mask opening. Therefore, the minimum gap (9 µm) and structure (14 µm) sizes for the metal 3 layer are larger relative to the metal 1 and metal 2 layer.

Based on the presented design rules for the fabrication processes and the desired trap geometry, the layout of the 2D twin trap including all functional layers was created.

4.2 Trap fabrication

The fabrication of the 2D twin trap is carried out at the cleanroom facilities of Infineon Technologies[1] on wafer level, using 8 " silicon wafers (200 mm diameter) as a substrate. Wafer level fabrication allows the simultaneous production of hundreds to thousands of devices on the same substrate, resulting in a time- and cost-saving production.

The fabrication of the 2D twin trap is based on a well-established technology. Wafers are processed via an automated process flow referred to as process of records (POR), which contains all individual fabrication and control steps. This POR is designed prior to the fabrication start of the ion trap and enables a fast and reliable production. In the following section the fabrication of the 2D twin trap is presented.

4.2.1 Silicon as basis material for ion traps

When considering different candidates as substrate material for ion traps, silicon is an interesting choice due to its wide range of possible processes that enable complex ion trap designs. Silicon is the most used basis material for semiconductor components, including microprocessors, memory chips and logic circuits [105]. It is the second most abundant element in the earth's crust, and thus available in almost unlimited

[1]The Infineon cleanroom in Villach has an area of around 23.000 m^2 and a cleanroom class of 1 - 1000, depending on the sub-area of the fab. The cleanroom class defines, how many particles with a diameter of 0.5 µm are allowed in a volume of 1 ft^3.

quantities. At room-temperature, silicon bonds with oxygen, forming silicon dioxide SiO_2, a mechanically and electrically stable insulator, suitable for electrical separation of the silicon substrate and conducting layers applied on top. Due to the numerous advantages and possible applications of silicon in semiconductor industry, there is a large tool park of different processes that enable complicated layer structures and chip layouts.

However, not only advantages in the manufacturing process, but also the requirements for material properties in relation to the ion trap performance must be taken into account. Common surface ion traps use RF voltages of around $100 - 200\,\mathrm{V}$ to confine ions. If RF leaks into the substrate, it will cause the trap to heat up. Moreover, a change in temperature affects the RF voltage gain by the resonator due to a shift of the resonance frequency, as the matching is no longer optimal. To compensate for a lower RF voltage gain, even more voltage has to be applied, which in turn causes the chip to heat up further.

The loss tangent describing the amount of electromagnetic energy dissipated in a material is given by

$$\tan\delta = \frac{1}{Q}, \tag{4.1}$$

with the quality factor Q. In a semiconductor, the loss tangent is defined by the following equation:

$$\tan\delta = \tan\delta_d + \frac{1}{\rho\Omega\epsilon_0\epsilon_r}. \tag{4.2}$$

Here, $\tan\delta_d$ represents the dielectric loss tangent, ρ is the resistivity, Ω the angular frequency (in this case the RF drive frequency), ϵ_0 the vacuum permittivity and ϵ_r the semiconductor's relative permittivity [107]. With an increasing resistivity of the material, the loss tangent decreases. Another mechanism producing RF losses is the generation of charge carriers by accumulation and inversion in the underlying substrate [108] when a typical voltage of 200 V is applied to a surface electrode. This effect is also present in substrates with a high resistivity. At room temperature, intrinsic silicon with a high resistivity has a loss tangent of around 1.5 at typical RF trap frequencies of around 20 MHz [107], which is still too high for a reliable ion trap operation.

There are two possibilities to circumvent this issue: first, the integration of a shielding layer helps reducing the dissipated energy from the RF electrode to the substrate. This needs an additional metal layer and adds complexity to the fabrication process. Moreover, an additional GND layer below the RF electrodes contributes to a higher trap capacitance, which can lead to higher RF losses and heating of the trap.

Second, the ion trap is operated at cryogenic temperatures. At temperatures lower than 25 K the charge carriers in silicon freeze out [107], and hence the resistivity of the substrate increases and RF losses are reduced.

Another interesting and commonly used substrate material for ion traps is fused silica. At room temperature, the loss tangent of fused silica is as low as $\sim 10^{-4}$ [109]. But, in semiconductor manufacturing facilities, most fused silica substrates are classified in a critical contamination class due to their sodium contents, that could contaminate other wafers. Moreover, because glass wafers are transparent, problems can arise with the automatic detection of the wafers in different process tools.

For the 2D twin trap fabrication, either a standard silicon substrate with $3\,\Omega\,\mathrm{cm}$ resistivity or a high-Ohmic, float-zone substrate with $\rho > 8\,\mathrm{k}\Omega\,\mathrm{cm}$ resistivity were chosen as wafer material. The ion traps are operated at cryogenic temperatures and the trap layout contains a shielding layer to reduce RF losses.

4.2.2 Basic fabrication steps

In total, the fabrication of the ion trap wafers consists of 103 process steps. This includes in-line reliability measurements and optical control steps, which make up for 20 % of all processes. The basic fabrication routine takes around 2 weeks for one wafer, which contains more than 700 chips.

In figure 4.8 the basic fabrication steps are depicted, corresponding to the layers given in table 4.2. After thermal oxidation of the substrate, the metal and oxide layers are deposited alternately. In the following, the structuring of the ion trap wafers is described in detail. This includes the process of optical lithography to create the etching pattern, as well as details on the used oxide and metal layers.

Optical lithography

All layers except the thermal oxide are structured by optical lithography followed by an etching step. Optical lithography consists of three consecutive steps: first, the wafer is coated with (radiation sensitive) photoresist. Second, a UV light exposure through a mask images the desired pattern on the wafer, followed by the development of the photoresist. For the patterning of all structural layers in the ion trap the resist is exposed with 365 nm UV-light in the so-called i-line [110]. The term i-line refers to a line in the emission spectrum of a mercury vapor lamp (in this case 365 nm), which is used for exposure in lithography.

There are two types of resist, referred to as positive and negative resist. A positive (negative) resist dissolves in the UV exposed (not UV exposed) area during development.

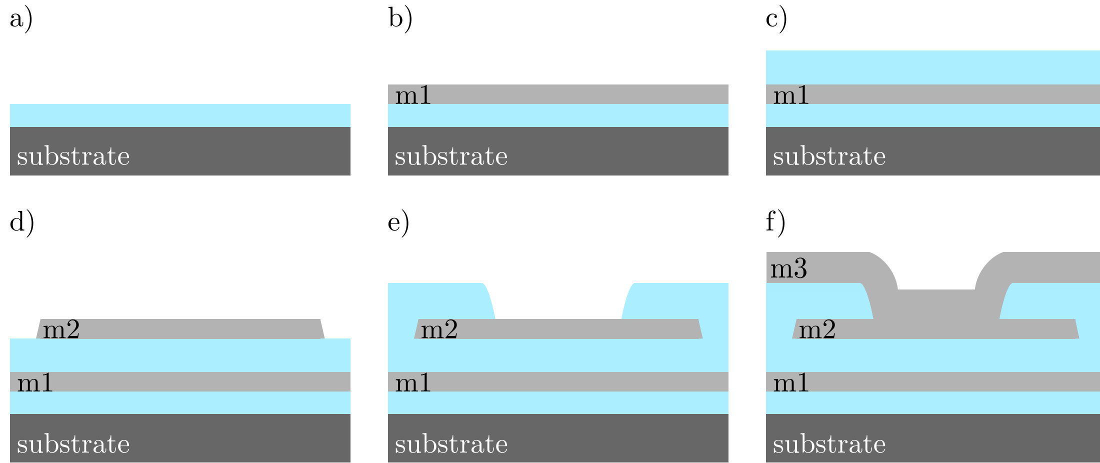

Figure 4.8: Basic fabrication steps for structuring the ion trap wafers on the silicon substrate (dark gray) at the position of a via. Metals are colored gray, oxide blue. a) Thermal oxidation, b) sputter deposition of metal 1 (m1), c) oxide deposition of imox 1, d) sputter deposition of metal 2 (m2), e) oxide deposition of imox 2 and etching, f) sputter deposition of metal 3 (m3) forming a via.

For the processing of the ion traps we exclusively use positive resist, which is spin-coated on the wafer. To achieve a homogeneous resist layer over the entire wafer covering all edges, the thickness of the resist is important, especially in the case of a high topology of the structured wafer, where we need a resist thickness of up to 4 µm. The thickness of the resist is mainly defined by the spinning speed and the viscosity of the resist and is optimized for every single layer.

After coating the wafer with resist, the desired structure is projected on the wafer via a quartz plate, in which the chip layout is defined by a chrome layer. This process is either performed with a 1:1 photo mask comprising the whole wafer layout, or with a reticle containing just one or a few chips, which is used with a step-and-repeat method. For fabrication of the 2D twin trap, only reticles are used that include up to 12 chips. The reticle is moved step by step over the wafer and is repositioned and aligned for each shot. With this method, adjustment errors due to temperature changes or distortion as present in a full-wafer mask is minimized. But, an increase in processing time has to be accepted since the reticle needs to be repositioned many times for one wafer.

To convert the resist structure transferred through UV exposure into an etching mask, a development step is performed, followed by a water rinsing to stop the process [105]. Subsequently, a post-exposure bake is conducted to cure the resist for the following process. The final step of the lithography is an optical inspection of the resist structures

to detect possible defects and to examine the alignment to the underlying layers.

Oxide layers

In the 2D twin trap, silicon oxide layers are integrated to isolate the substrate from the first metal layer and to separate the three metal layers from each other. Depending on the underlying substrate, there are two ways to create an oxide layer in semiconductor fabrication: thermal oxidation and oxide deposition. Bare silicon as substrate allows for a thermal oxidation, resulting in a pure SiO_2 layer. This process needs high temperatures of around 1000 °C to heat up the silicon surface. The oxide growth rate is restricted due to the fact, that the oxygen has to diffuse through the already existing oxide layer until reaching the silicon below. Therefore, to achieve thick oxide layers, long process times are necessary. A rough estimation gives a reduction in layer growth proportional to the square root of time [105]. Nevertheless, advantages of thermal oxide are a low defect density and low interface roughness. Moreover, high breakdown voltages can be achieved due to the high density of the layer.

If an oxide is required on top of a metal layer, no thermal growth can take place because no silicon is present in the underlying layer. Thus, silicon has to be supplied in addition to the oxygen. An often used oxide deposition method is tetraethyl orthosilicate (TEOS, $SiO_4C_8H_{20}$) deposition [105]. TEOS is an ethyl compound that is fluid at room-temperature, containing both oxygen and silicon. Heating up the fluid to the gas phase, the ethyl groups split, so that SiO_x with $x \approx 2$ is deposited on the wafer surface. Compared to thermal oxide, the carbon content is higher, leading to a lower refraction index [105]. However, the process temperature related to the wafer is much lower, so that processing is possible even if metal layers with a lower critical temperature have already been deposited on the wafer. In this context, the critical temperature of a metal defines the maximum temperature allowed for further processing to prevent damaging of thin layers.

The bottom oxide of the 2D twin trap is grown thermally on the silicon substrate. The two imox layers need to be deposited, due to the underlying metal surface and the restricted maximum processing temperature of 420 °C when using AlSiCu for metal layers. The imox layers need to support vias for an electrical connection in between two metal layers. These vias are realized through plasma etching leading to a funnel-shaped aperture in the oxide, see figure 4.9. This enables a sufficient coating of the via sidewalls given by the metal deposited above.

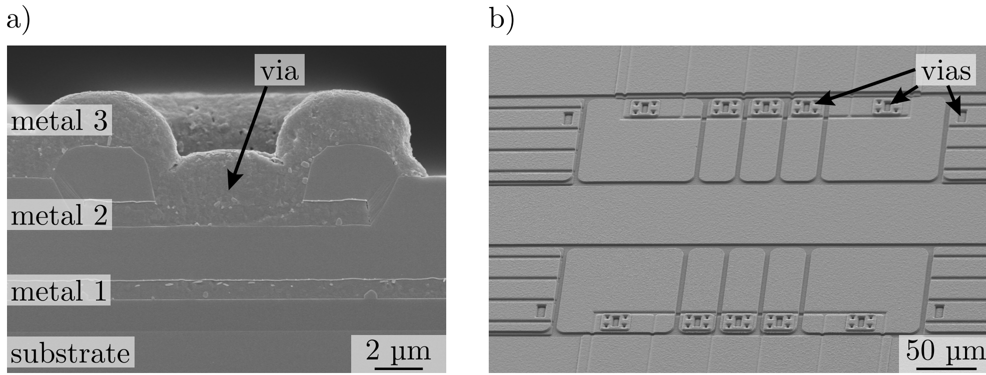

Figure 4.9: Scanning electron microscopy (SEM) image of the ion trap. a) Cross section of the layer stack at the position of a via between metal 2 and metal 3. Unlabelled, gray layers are isolating oxide. b) Central zone of the ion trap in 45° angle. The segmented electrodes are connected to underlying metal layers by multiple vias.

Metal layers

The three AlSiCu metal layers of the 2D twin trap are created via sputter deposition. In this process, a target made of the desired metal material is bombarded with highly accelerated ions. Thus, atoms or molecules from the target are ejected, move with an energy of $1 - 10\,\mathrm{eV}$ and subsequently deposit on the wafer surface. Since the sputter process takes place at higher pressure ($\sim 10\,\mathrm{Pa}$) compared to evaporation, the mean free path of the particles is in the millimeter range. For this reason, the particles will change their direction multiple times due to collisions with gas molecules, before depositing on the wafer. Thus, they hit the wafer surface at different angles, resulting in the coating of vertical sidewalls. This enables the electrical connection of metal layers through vias. Sputter deposition allows for a larger layer thickness compared to evaporation methods, which are limited by the amount of material that can be deposited in one process run. Moreover, sputter deposition allows for a better control of the layer thickness and results in a higher uniformity of the deposited layer [105].

The first two metal layers (metal 1 and metal 2) are structured via anisotropic plasma etching. Due to the larger layer thickness of $2\,\mu\mathrm{m}$ of the metal 3 layer, the first traps were processed with an isotropic wet etch for this layer, before a working plasma etch was developed. The two etch techniques can be used to create two different gap widths in between the electrodes of $5\,\mu\mathrm{m}$ and $9\,\mu\mathrm{m}$ for a plasma and a wet etch, respectively, as depicted in figure 4.10. Because stray charges in dielectrics lead to increased micromotion of the ion, smaller gaps between electrodes help to reduce the

amount of oxide in direct line of sight to the ion.

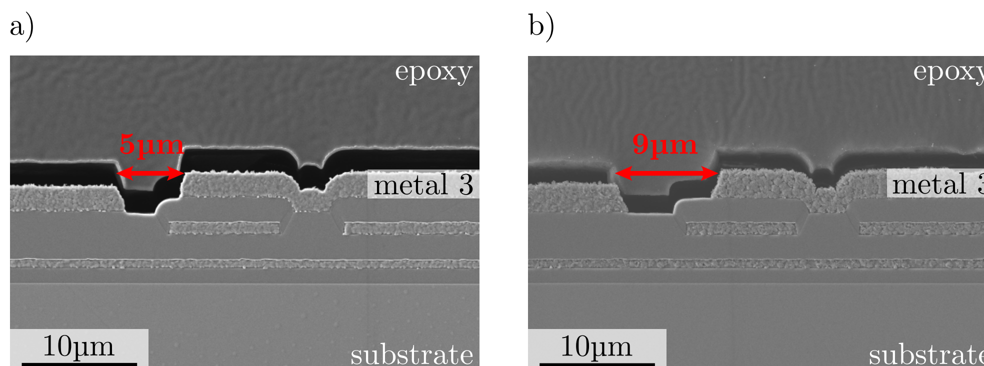

Figure 4.10: SEM image of the ion trap cross section. Metal layers are visible in light gray, separated by oxide layers (dark gray). Before the chips were broken and polished, they were embedded in epoxy. The epoxy layer detached from the ion trap chip, visible as a dark area. The metal 3 layer is structured with an a) anisotropic plasma (dry) etch and b) isotropic wet etch. The different etching technique results in gaps between the electrodes of 5 µm and 9 µm, respectively.

4.2.3 Fabrication changes for multiple trap generations

During characterization of the first 2D twin traps in the experiment, relatively high stray electric fields were detected at the ion's position in the first characterized ion traps, as described in detail in refs. [29, 111]. Therefore, two improvements on the fabrication process were introduced to reduce stray fields generated on the ion trap surface. An under etch of the trap electrodes leads to a recess of the gap oxide, thus minimizing the amount of exposed oxide and thus the effects of stray electric fields at the ion's position. Additionally, the AlSiCu electrodes were coated with a thin layer of gold.

Underetched electrodes

In the first iteration of the 2D twin trap the oxide in the gaps between the trap electrodes is in direct line-of-sight to the trapped ions. During trap operation with laser light, stray charges are created at the dielectric surface, causing stray electric fields. Such static electric fields induce micromotion and heating of the ions, and results in changes in the ion-laser interaction [112]. To circumvent this effect, an additional oxide etch was introduced to the fabrication routine. An isotropic wet etch with high selectivity to aluminum is performed to etch both imox layers down to the metal 1 shield layer,

therefore recessing the oxide below the electrodes, as shown in figure 4.11.

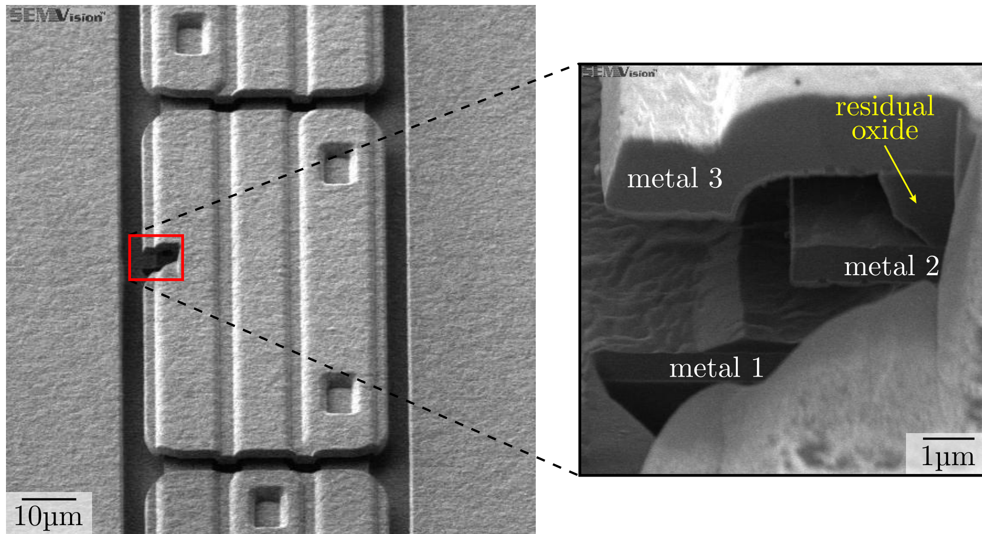

Figure 4.11: SEM image of under etched electrodes to reduce the amount of oxide in direct line of sight to the ion. A cross section of the layer stack can be generated by a focussed ion beam cut, visible as a hole in the left picture (red frame). The cross section of the ion trap is shown in the right SEM image, taken in a 45° angle for better visualization. The oxide is etched down to the metal 1 shield layer.

Gold as electrode surface material

Another drawback of the first 2D twin trap is the electrode material, an alloy of aluminum, silicon and copper. Aluminum as metal material is advantageous since it is compatible with standard CMOS microfabrication. However, the growth of native oxide on the aluminum surface when exposed to air is a possible source of stray-electric field noise [99]. A commonly used surface material in ion traps is gold, which features a high conductivity. Moreover, no native oxidation occurs when exposed to air. Nevertheless, the poor compatibility within a CMOS production line to avoid contaminations of other wafers limits the possibilities of including a gold coating for the ion traps in our process.

To avoid contamination of other productive wafers, a gold coating of the ion trap wafers has to be performed as the last process step. The wafer is evaporated with a stack of 50 nm titanium, 100 nm platinum, and 200 nm gold. Here, titanium serves as an adhesion layer and platinum as a diffusion barrier to avoid migration of gold atoms in underlying layers [113]. The evaporated gold layer covers the whole wafer surface. Because the oxide in the gaps between electrodes is under etched in the previous process

step, shorts between electrodes are avoided. Thus, no additional structuring of the gold layer is required. A schematic cross section of the ion trap before and after adding the under etch and gold evaporation is shown in figure 4.12.

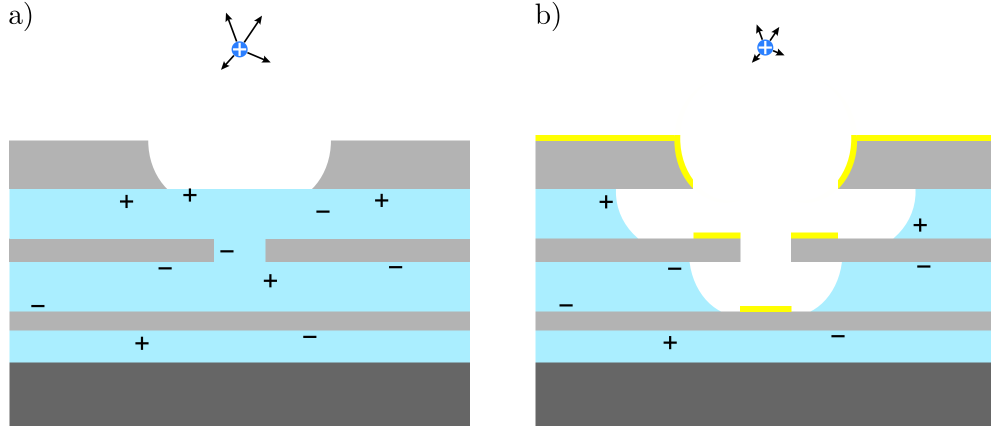

Figure 4.12: Schematic layer cross section of the 2D twin trap. a) Layer cross section of the first 2D twin trap with exposed oxide (light blue) in the gaps between electrodes (light gray) in direct line of sight to the ion (blue circle). Spatial fluctuations of stray charges in the dielectric (marked with black +/-) increase the ion's micromotion. b) Layer cross section of the 2D twin trap with improved fabrication, including under-etched electrodes, which provide a shielding of stray charges in the oxide. A coating of the AlSiCu electrodes with gold (yellow) reduces the risk of adsorbants or native oxide on the aluminum.

4.2.4 Dicing

To isolate the single ion trap chips on the wafer, a dicing process is performed. In semiconductor industry, a variety of methods for separating single chips on a wafer is available, such as laser cutting [114], stealth dicing [115], plasma dicing [116], and mechanical dicing [117]. At the Infineon production facilities in Villach, mechanical dicing is the preferred method for separating semiconductor chips, hence we implemented this process for the 2D twin trap. A grinding wheel containing diamonds is moved over the wafer at high rotational speed. The width of the scribe line needs to be defined already while generating the wafer layout to facilitate the required space for the dicing process. Dicing marks are placed in this area to allow for an automatic alignment of the dicing tool. Typically, also the alignment marks used to align the structuring of different layers as well as measurement targets are placed in the area used for dicing. Depending on the wafer thickness and material a suitable sawing blade is chosen.

Before dicing, the whole wafer is fixed on a UV-releasable tape[2] to maintain the position and location of individual chips during and after dicing. Then, a full cut of the wafer is performed down to the underlying foil that holds the chips on the wafer. During dicing a jet of fluid ensures that dicing debris are rinsed off immediately. This fluid mainly consists of water with a small amount of an additional cleaning agent StayClean-F[3], acting as a surfactant (surface active agent). Silicon particles detached through dicing tend to deposit in the slightly acidic water used during dicing, especially on topological edges. To prevent this, the surfactant forms a polar bond with the wafer surface creating a protective layer. This procedure also inhibits corrosion of aluminum and copper [118]. After dicing, the wafer is rinsed with de-ionized water and subsequently exposed with UV light to weaken the adhesion of the single chips to the foil. This simplifies the manual detachment of chips with tweezers. Figure 4.13 shows a taped wafer fixed in the dicing frame as well as a zoom-in of the diced wafer.

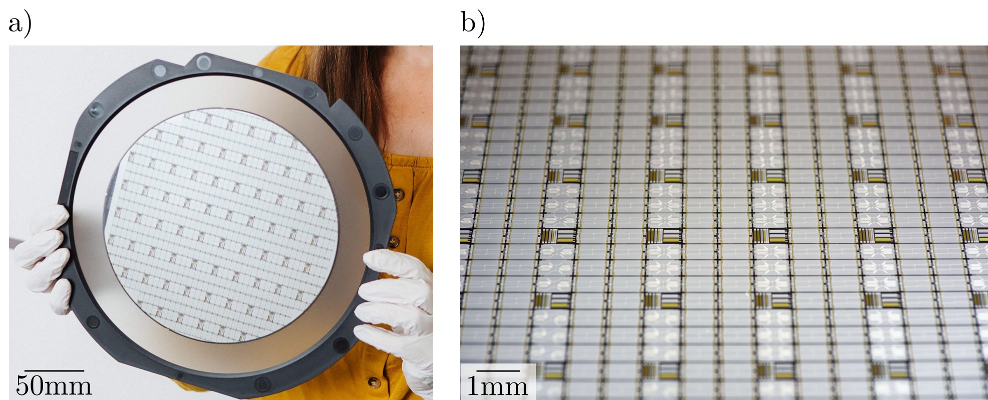

Figure 4.13: a) 8 ” diameter ion trap wafer after dicing fixed on a UV-releasable tape. b) Diced on trap chips still fixed on the tape. Different trap designs and test structures are fabricated on the same wafer.

4.2.5 Packaging

The first ion traps fabricated at Infineon Technologies were delivered to the university as bare dies. Glueing of the trap to the carrier printed circuit board (PCB) as well as the electrical connection to the carrier PCB, filterboard and RF resonator through wire bonding was manually performed in the university's cleanroom. This procedure is not time-efficient, since it takes at least one day to produce a fully wirebonded ion trap. Moreover, the reliability of the wirebonded traps is limited due to possible human errors

[2]LINTEC, D497 or D495H
[3]StayClean-F, DISCO, water soluable additive

in manual handling and processing. Therefore, an industrial packaging of the ion traps was developed, which is carried out at the back-end facilities of Infineon Technologies in Regensburg.

The carrier PCB creating the electrical connection to the voltage supply is specially designed to fit the 2D twin trap. The PCB is a standard 101 pad land grid array (LGA) similar to socket solutions for other state-of-the-art ion traps [119], and is made of Rogers 4350B with copper metallization. The copper has an electroless palladium / immersion gold (EPIG) coating that is nickel-free and ideal for high frequency applications. The ion trap is glued on the PCB with a conductive Infineon proprietary glue with a silver content $> 90\,\%$ after curing. The ion trap chip is then wirebonded to the PCB with $25\,\mu m$ thick gold wires via a fully-automatic ball-bonding process. Each bond pad is connected with two wire bonds for redundancy. The assembled ion traps on carrier PCB are then shipped to the university. Pictures of the assembled ion trap are shown in figure 4.14.

Combined with the automated packaging process, an ion trap socket for mounting in the vacuum chamber was developed compatible with the standardized Infineon carrier PCB. This socket allows for an easy and fast sample change, shows good thermal anchoring and enables the integration of electronics close to or directly on the ion trap chip. Patenting of this ion trap socket is ongoing at the time of writing of this thesis. Details on the layout, materials, as well as an electrical and thermal characterization will be described in [120].

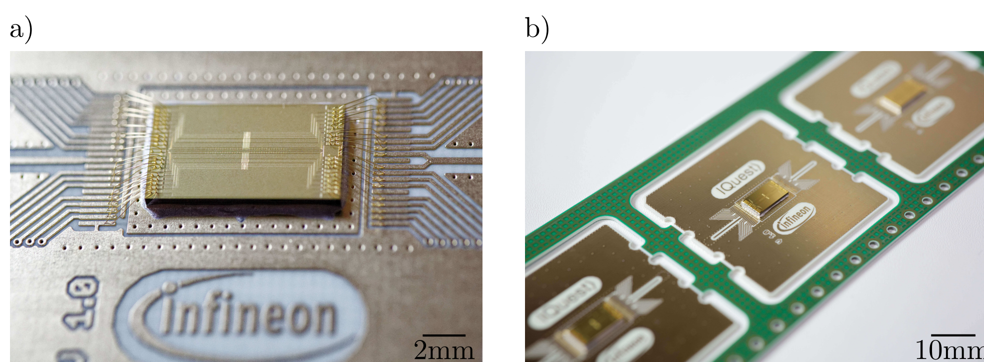

Figure 4.14: Industrial ion trap package accomplished by Infineon Technologies. a) Ion trap with double wire bonds glued to the carrier PCB. b) Multiple wirebonded ion traps on carrier PCBs still fixed in the lead frame (structural support layer to provide stability during manufacturing operations and transport).

4.3 Electrical characterization

To verify electrical functionality of the ion trap, several tests were performed on the ion traps themselves as well as on dedicated test structures. These test structures are fabricated on the same wafer as the ion traps, sharing the same materials, layer properties and processing steps. Therefore, measurements on the test structures are a suitable method to characterize properties of the ion traps, such as resistances of metal layers and vias. Moreover, breakdown voltages between RF electrodes and neighboring DC and GND electrodes on the ion trap were measured at room temperature and cryogenic temperatures. Finally, the capacitance of the RF electrodes to the metal 1 shield layer was investigated.

4.3.1 Resistance of metal layers and vias

To minimize heating of the ion trap due to Johnson Nyquist noise (see section 3.2.1), leads to the electrodes are designed to be as wide and thick as possible to reduce their resistance. In the 2D twin trap, several segmented DC electrodes are routed through relatively thin metal lines of $10 - 20\,\mu\text{m}$ width and $1\,\mu\text{m}$ thickness. These metal layers are connected through vias with a cross-sectional area of $4 \times 4\,\mu\text{m}^2$ (metal 1 to metal 2) and $6 \times 10\,\mu\text{m}^2$ (metal 2 to metal 3).

The resistance of the three metal layers and both vias was measured at room temperature and cryogenic temperature (20 K) in a vacuum environment. Meander test structures in each metal layer with a length of 65.5 mm and a width of 14 µm were used to determine the metal resistance. From the measured resistances at room temperature, the resistivity of the metal layers is calculated, giving values of $(2.2\ \text{-}\ 2.7) \times 10^{-8}\,\Omega\,\text{m}$. The calculated resistivity values are listed in table 4.4. These values are comparable to similar aluminum alloys found in literature for bulk resistance [121]. The different values for the three individual layers are caused by the additional 25 nm TiN layer on top of metal 1 and metal 2. The higher resistivity of TiN [122] increases the resistivity of the AlSiCu + TiN stack. At a temperature of 20 K the resistivity drops to around 10 % of the room-temperature values, agreeing well with analysis found in literature [123].

To determine the via resistance, a series of 30 identical, interconnected vias were used. For one via connecting two metal layers a resistance of (20-50) mΩ was measured at room temperature. Again, the resistance at 20 K drops to around 10 % of the room-temperature value, resulting in a resistance of only a few milli Ohms per via. In the ion trap, all electrodes are connected with at least two vias to further reduce the resistance. Table 4.5 lists the measured values for vias connecting different metal layers. The

Table 4.4: Resistivity ρ of the individual metal layers.

metal layer	ρ (Ω m) at 300 K	ρ (Ω m) at 20 K
m3	$2.278(1) \times 10^{-8}$	$2.41(2) \times 10^{-9}$
m2	$2.703(3) \times 10^{-8}$	$2.58(3) \times 10^{-9}$
m1	$2.524(4) \times 10^{-8}$	$2.54(1) \times 10^{-9}$

discrepancy between different via types is caused by the different metal thickness: a thicker metal layer leads to a stronger coverage of the via side walls, resulting in a lower resistance.

Table 4.5: Resistance R_{via} of one via connecting individual metal layers.

via connecting	R_{via} (mΩ) at 300 K	R_{via} (mΩ) at 20 K
m2 to m1	51.91(2)	6.52(3)
m3 to m2	23.31(1)	2.70(2)
m3 to m1	37.17(1)	4.94(4)

To determine the Johnson Nyquist noise induced by the trap electrodes, the leads routing the segmented DC electrodes in the metal 2 layer to the bond pads are used. These leads have the highest resistance compared to all other metal structures on the trap chip. A resistance of $5\,\Omega$ for the leads at room temperature and $0.5\,\Omega$ at 20 K is calculated with the measured resistivity values given in table 4.4. We estimate the resistance of the wirebonds connecting the bond pads on the trap chip with the carrier PCB to be on the order of a few tens of milli Ohms [124] at room temperature and therefore negligible compared to the lead resistance. With a characteristic distance of $\delta_{c,z} = 2.2\,\text{mm}$ [79] the amount of electric field noise is $S_E \sim 1.7 \times 10^{-14}\,\text{V}^2\,\text{Hz/m}^2$ at room temperature for the axial direction, following equation (3.5). With a secular frequency of $\omega_z = 2\pi \times 1\,\text{MHz}$ this results in a heating rate of $\Gamma_{\text{h,300K}} = 2.5\,\text{q/s}$. At a temperature of 20 K, the heating rate reduces by around two orders of magnitude to $\Gamma_{\text{h,20K}} = 0.015\,\text{q/s}$ due to the lower metal resistivity. Similarly, the heating rate for the radial modes is calculated for one direction, using a characteristic distance of $\delta_{c,r} = 0.9\,\text{mm}$ and radial frequency of $\omega_r = 2\pi \times 3\,\text{MHz}$. The outcome is a slightly higher heating rate of $\Gamma_{\text{h,300K}} = 4.8\,\text{q/s}$ and $\Gamma_{\text{h,20K}} = 0.033\,\text{q/s}$ at room temperature and cryogenic temperature, respectively. Therefore, no significant ion heating in the trap due to Johnson Nyquist noise is expected during trap operation at cryogenic temperatures.

These calculated values for the heating rate generated by Johnson Nyquist noise are later compared to measurements performed on the ion trap in the experiment, see section 4.5.4.

4.3.2 Breakdown tests

The metal layers of the 2D twin trap are separated by 2.2 µm thick dielectric layers of deposited silicon dioxide. Applying a high voltage to the RF electrodes leads to leakage currents through the dielectric and in the worst case to a full breakdown [125] destroying the ion trap. Hence, it is important to investigate the dielectric strength of the oxide layers to define a maximum voltage applicable to the trap without risking damage. A first measurement of the breakdown voltage was performed on test structures with parallel metal structures of the size 700 µm $\times$ 3500 µm in each metal layer to form a plate capacitor. These measurements were conducted on eight samples with a DC voltage at room-temperature and atmospheric pressure. A mean breakdown voltage of 1.21(5) kV for the dielectric between metal 1 and metal 2 was measured. The breakdown voltages of all samples are shown in figure 4.15. The expected breakdown voltage for an ideal thermal oxide is given by 1 V/nm based on empirical values from Infineon. In the case of the plasma oxide deposited on the ion trap wafers, this value reduces to $\sim$ 0.55 V/nm. Measured breakdown voltages between metal 2 and metal 3 as well as between metal 1 and metal 3 were limited by surface flash-over and arcing [126]. The flashover was located in the area of the bond pads, where the distance to the leads is only 25 µm, reducing the breakdown voltage to 447(4) V and 446(8) V, respectively.

Another series of breakdown test was conducted on the ion traps. To simulate a realistic experimental environment, the tests are performed in vacuum inside the cryostat at Kompetenzzentrum für Automobil- und Industrieelektronik (KAI). At 20 K, a breakdown voltage of $\geq$800 V was determined for various combinations of RF and DC/GND electrodes. Moreover, the breakdown voltage in vacuum at room temperature was investigated, resulting in similar values of $\geq$800 V. This indicates no limitation by surface-flashover in a vacuum environment. In table 4.6 the results of the different breakdown tests are summarized.

The RF voltage applied to the ion trap during operation is in the range of $150-200$ V. Although the RF breakdown voltage might differ from the DC breakdown voltage, we expect the layer stack of the ion trap with 2.2 µm imox layers to be compatible with the experiment due to the high DC voltages that can be applied to the trap.

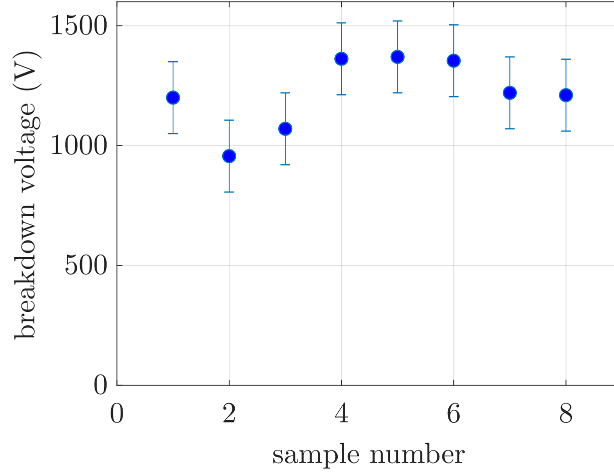

Figure 4.15: Dielectric breakdown voltage measured on test structures between the metal 1 and metal 2 layer for eight samples. The measurement was conducted at room temperature and atmospheric pressure. The mean breakdown voltage of the eight measured samples is 1.21(5) kV.

4.3.3 Capacitance measurements

To avoid RF losses in the silicon substrate, the ion trap has an additional shielding layer in metal 1 connected to GND. The RF electrodes and this GND layer form a plate capacitor, separated by only 4.4 µm (in the interaction zone 2.2 µm) of deposited oxide. This capacitance influences the resonance frequency of the RF resonator, therefore the knowledge about the trap capacitance is important to design a suitable RF resonator. The capacitance analysis was performed on ion traps with 80 µm ion-surface distance, fabricated on either standard silicon substrate with $\rho = 3\,\Omega\,\mathrm{cm}$ or a high-Ohmic silicon substrate with $\rho > 8\,\mathrm{k}\Omega\,\mathrm{cm}$, see section 4.2.2. The capacitance between the outer RF electrodes and the inner RF electrode to GND as well as the coupling capacitance between

Table 4.6: Breakdown mechanism for different environments and temperatures between RF and DC/GND electrodes of the 2D ion trap.

environment	temperature	V_{break} (V)	mechanism
atmospheric pressure	300 K	~ 450	surface flashover
vacuum	300 K	≥ 800	dielectric breakdown
vacuum	20 K	≥ 800	dielectric breakdown

the two RF electrodes was measured in ambient conditions and a dark environment to avoid light-induced stray charges. Figure 4.16 shows a schematic of the capacitances present in the ion trap. The measured values are $C_{og} = 38.00(1)$ pF (36.36(3) pF) for the outer RF, and $C_{ig} = 6.40(1)$ pF (4.92(1) pF) for the inner RF to GND on the standard silicon substrate (high-Ohmic silicon substrate). These values are much higher than single-layer traps, but still comparable to other ion traps with multiple metal layers [90].

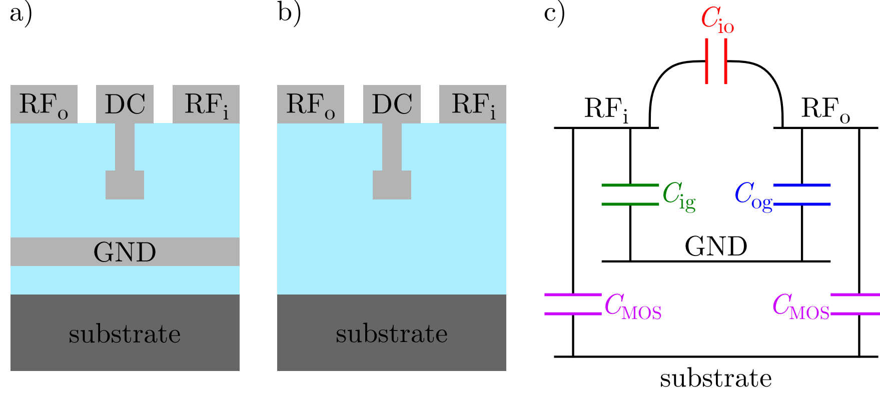

Figure 4.16: a) Schematic layer cross section of the 2D twin trap in the central trap area with metal electrodes (bright gray), isolating oxide (blue) and substrate (dark gray). b) Schematic layer cross section of the 2D twin trap in the bond pad area without shielding GND layer. c) Schematic of the capacitance between the two RF electrodes (C_{io},red), the inner RF electrode to GND (C_{ig}, green), the outer RF electrodes to GND (C_{og}, blue), and a MOS capacity between the RF electrodes and the silicon substrate (C_{MOS}, purple) in the 2D twin trap.

Stray light or lasers can induce charge carriers in the substrate, changing the trap capacitance. Thus, to evaluate the influence of stray light on the ion traps, a measurement of the capacitance was performed during light exposure. The RF capacitance of the ion trap was measured with a bias voltage applied to the RF electrode, while the GND electrode is connected to GND. The bias voltage is tuned from -100 V to 100 V. A drop in the capacitance of a few pico Farad was observed for the high-Ohmic silicon substrate compared to the standard substrate when exposed to white light, see figure 4.17. This can be explained by the contribution of a MOS (metal-oxide-semiconductor) capacitor, which is created by the RF electrode and the silicon substrate in the area of the bonding pads. In this area, the GND shield of the metal 1 layer is omitted to avoid shorts during the wirebonding process, as described in detail in section 4.5.1. If the trap is exposed to light, charge carriers are generated by accumulation and inversion in the

underlying substrate [108], thus preventing depletion of the MOS capacitor. At lower voltages up to 40 V, the charge carriers at the interface are depleted resulting in a lower capacitance. This effect only occurs with the high-Ohmic substrate. The results of the capacitance measurements are listed in table 4.7. Thus, for the ion traps presented in this thesis only a standard silicon substrate was used.

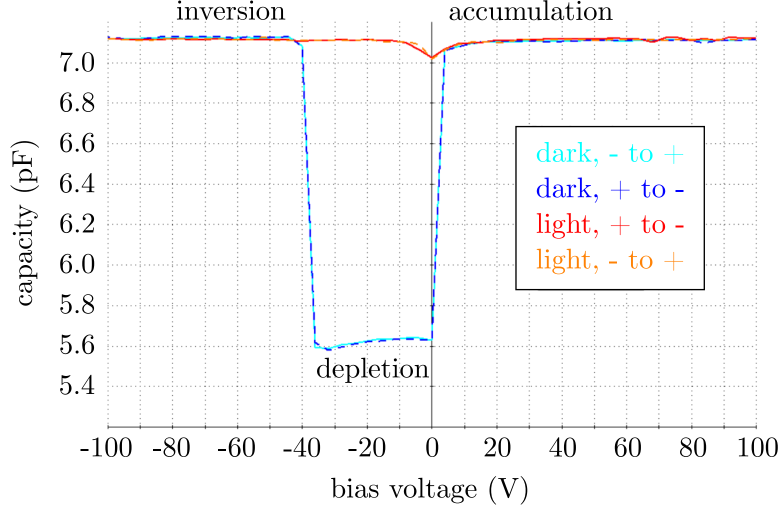

Figure 4.17: Capacitance of RF to GND for the 2D twin trap while applying a bias voltage to the RF electrode and connecting the GND electrode to GND. The ion trap shows a behavior as a MOS capacitor when exposed to light. Depletion is only observed in a dark environment up to a voltage of around 40 V, resulting in a lower capacitance. Note, that the sign of the bias voltage is inverted due to restrictions in the measurement setup.

Table 4.7: Capacitance of the outer RF electrode (C_{og}) and inner RF electrode C_{ig} to GND for a standard $\rho = 3\,\Omega\,\mathrm{cm}$ silicon substrate and a $\rho > 8\,\mathrm{k}\Omega\,\mathrm{cm}$ silicon substrate. For an estimation of the influence of stray light, the trap was illuminated in one measurement.

	C_{ig} (pF)	C_{og} (pF)
standard substrate, dark	6.40(1)	38.00(1)
standard substrate, light	6.41(1)	38.02(1)
high-Ohmic substrate, dark	4.92(1)	36.36(3)
high-Ohmic substrate, light	6.33(1)	41.01(1)

Moreover, the coupling capacitance between the two RF electrodes is measured,

resulting in a value of $C_{\text{io}} = 0.06(1)\,\text{pF}$. An explanation for this small value is the shielding created through DC and GND electrodes located between the two RF rails. With the measured values of the trap capacitance, the RF resonator can be designed for a sufficient voltage gain to provide an RF voltage of 180 V.

4.4 Experimental setup

The 2D twin trap presented in this thesis was operated at cryogenic temperatures in ultra-high vacuum (UHV). Thus, a cryogenic setup was used, which was originally set up by Michael Niedermayr at the University of Innsbruck. Details on the setup are given in his PhD thesis [127]. In the following section, the experimental setup consisting of the cryostat connected to the vacuum chamber, the ion trap setup including the electronics to operate the ion trap, the necessary optical setup as well as the experiment control are described.

4.4.1 Cryostat and vacuum chamber

For cooling the ion trap inside the vacuum chamber, a closed-cycle Gifford McMahon cryostat is used. The vacuum chamber made of stainless steel is formed by two parts providing CF (ConFlat) flanges: a home made CF160 full nipple and a CF160 octagon chamber. In fig. 4.18 a cross section of the cryostat and the octagon with viewports is depicted. Two cold stages (50 K-stage and 10 K-stage) connected to the vacuum chamber are employed to reach the final base temperature of around 10 K necessary for a reliable ion trap operation. Attached to each stage is a radiation shield (50 K-shield and 10 K-shield, respectively) made of 5 mm copper, creating the cryogenic environment for the trap setup. These shields reduce the black-body radiation and moreover serve as a target for background molecules to freeze out far away from the ion trap. The largest cryogenic pump of the system is given by activated charcoal, placed in a container fixed at the 10 K-shield. The charcoal also provides a good vacuum due to its large surface area, to which gas molecules can adsorb.

The electrical leads inside the cryostat are realized by 20 coaxial cables made of stainless steel that are guided through electric BNC feedthroughs on the CF160 full nipple to link them to the electronics outside the cryostat.

Laser access to the ion trap is realized through viewports incorporated in the octagon and windows in the two heat shields equipped with anti-reflection coatings. The lasers for cooling and photoionization processes are coupled into the vacuum chamber perpendicular to the 729 nm qubit laser, see figure 4.18b. A detailed description of the optical setup is given in section 4.4.3. An additional window on the bottom flange of the

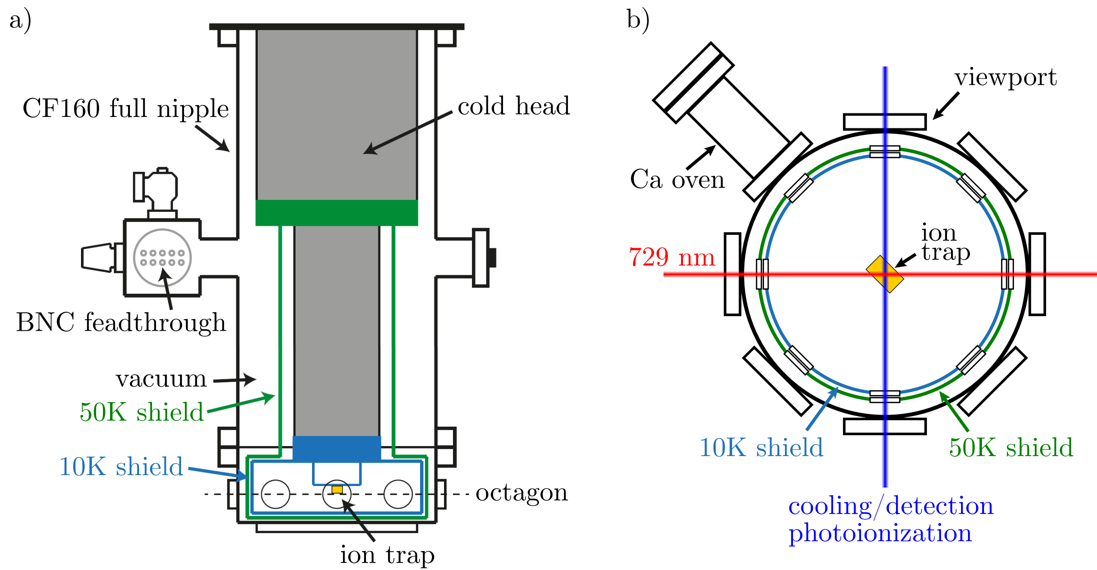

Figure 4.18: (a) Cross section of the cryostat. The vacuum chamber is formed by a CF160 full nipple and the octagon. The ion trap is enclosed by a 10 K shield (blue) and a 50 K shield (green) connected to the respective cold stages, and is thermally bonded to the cold head. BNC feedthroughs provide the electrical connection into the cryostat. (b) Cross section of the octagon. Viewports on each side of the octagon and windows in the heat shields allow for laser access. Cooling and photoionization lasers enter the cryostat perpendicular to the 729 nm qubit laser, both in 45° angle with respect to the quantization axis. The Ca oven is attached to one viewport for loading Ca atoms. Figure adapted from [127].

octagon allows for detecting the ion's fluorescence for state discrimination. A stream of atomic calcium is provided by a Ca oven attached to one of the CF40 flanges of the octagon and holes in the two radiation shields. Two pairs of electromagnetic coils are installed on four sides of the octagon to create the electromagnetic field to define the ion's quantization axis to be 45° relative to the laser beams.

4.4.2 Trap setup

For optimal cooling of the ion trap, a good thermal bond of the trap setup to the cryostat cold head is necessary. Therefore, the PCB carrying the ion trap (carrier PCB) is clamped on a copper base that is directly mounted on the 10 K stage of the cold head. Low-pass filters for the DC lines and an RF resonator, which are both located on

additional PCBs, are electrically connected to the trap by wire bonds. A temperature sensor (diode sensor) is integrated to determine the temperature as close as possible to the trap. In figure 4.19, the trap setup inside the cryostat is depicted.

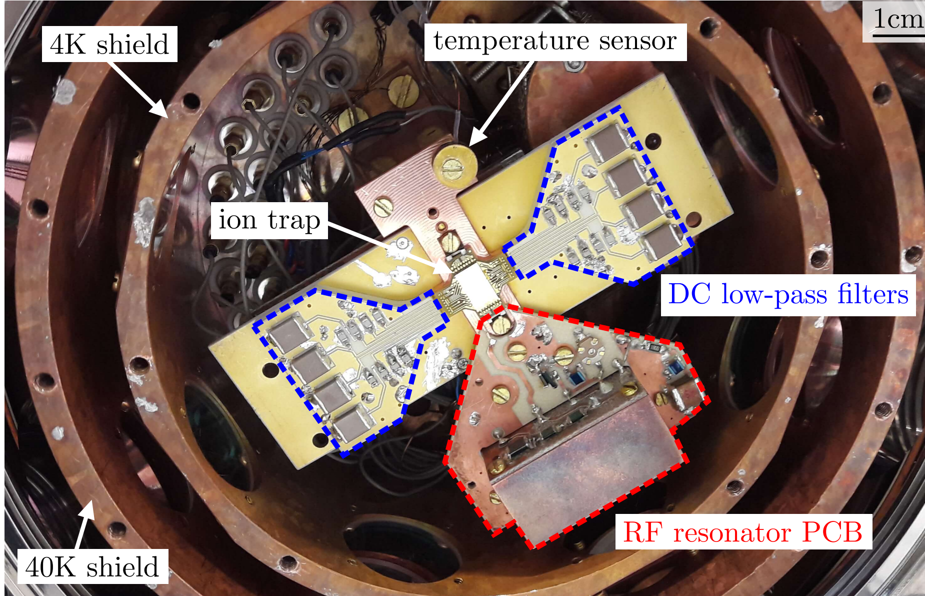

Figure 4.19: The ion trap assembled in the cryostat. Second order low-pass filters (blue) filter noise in the DC channels. An RF resonator (red) is used to amplify the RF voltage inside the vacuum chamber. A temperature sensor is integrated close to the ion trap.

RF resonator

To confine ions in microstructured surface traps, RF voltages of around 200 V at frequencies around $15 - 50$ MHz are necessary. To reduce the capacitance of the wires, the RF electronics are placed as close as possible to the ion trap [128, 129]. Thus, the RF voltage is amplified by a resonator directly connected to the carrier PCB of the ion trap.

The RF circuit consists of three main functional parts as shown in figure 4.20. A matching network is used to match the impedance of the RF circuit to the 50 Ω supply line to the signal generator. The matching consists of an inductance L_{m} and a variable capacitor C_{m}.

An RLC circuit forms the resonator to amplify the RF voltage needed for trap operation. A home made coil gives an inductance L_{r} and the resistance R_{r} is mainly given by the coil's resistance. The capacitor C_{trap} is defined by the trap itself, mostly

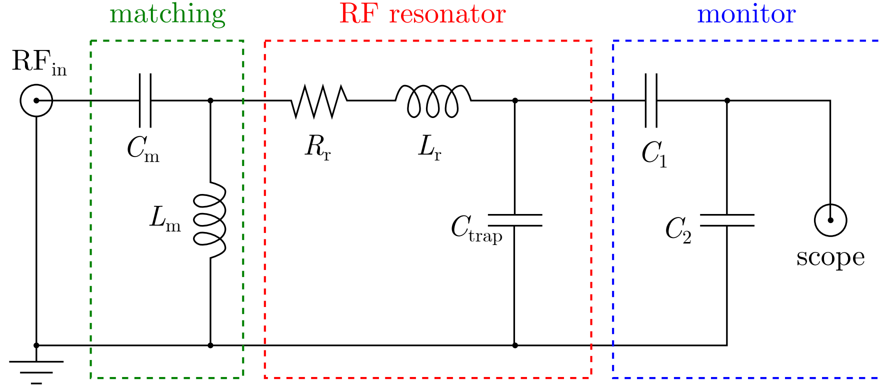

Figure 4.20: Schematic of the electrical circuit for the RF. A matching unit (green, $L_m = 1\,\mu H, C_m = 8 - 50\,pF$) serves for impedance matching to the $50\,\Omega$ supply line. The cap divider ($C_1 = 5\,pF, C_2 = 100\,pF$) of the monitor unit (blue) is used to track the voltage applied to the RF electrode. The RF voltage is enhanced with an LC resonator (red) including the trap itself as a capacitor ($C_{trap} = 40\,pF$) and a handmade coil-inductance ($L_r = 900\,nH, R_r = 0.46\,\Omega$).

by the capacitance between the RF electrode and the GND electrode on the trap. The resonance frequency of the RLC resonator

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{4.3}$$

is dependent on the inductance and capacitance of the circuit. A measure of the performance of the resonator is given by the quality factor Q described by

$$Q = \frac{2\pi f_0 L}{R} = \frac{1}{R}\sqrt{\frac{L}{C}}. \tag{4.4}$$

This parameter is proportional to the resonator's voltage gain, thus defines the enhancement of the RF source voltage.

For monitoring the voltage applied to the RF trap electrode a capacitive voltage divider is added to the circuit. Two capacitors C_1 and C_2 with $C_1 \ll C_2$ are placed in parallel so that the influence of the coaxial cable to the oscilloscope is negligible.

Depending on the geometry and fabrication, different ion traps also come with different trap capacitances. Hence, for every new ion trap the RF circuit needs to be adapted by changing the coil inductance and the matching for an optimal resonator operation regarding resonance frequency and RF voltage gain.

DC filters

To ensure high-fidelity quantum operations, a low level of electrical noise is required. For this reason, first order RC filters are used as low-pass filters for the DC lines providing the DC trap voltages. In figure 4.21, a schematic of the electrical circuit of a single DC line is shown. With a resistance of $R_f = 100\,\Omega$, and two capacitors of $C_{f,1} = 330\,\mathrm{nF}$ and $C_{f,2} = 470\,\mathrm{pF}$ placed in parallel, a cut-off frequency of $f_c = 4.8\,\mathrm{kHz}$ is achieved. This leads to a calculated noise reduction of 50 dB at 1 MHz.

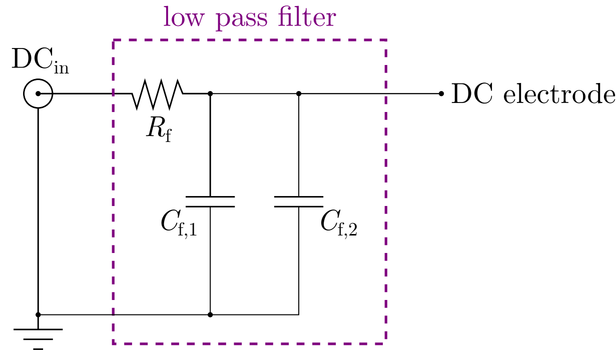

Figure 4.21: Schematic of the electrical circuit for one DC electrode with a first-order RC low-pass filter.

Trap mounting

The first generation of ion traps fabricated at Infineon Technologies were delivered as bare dies to the University of Innsbruck. The ion traps were prepared for mounting in the cryostat in the university's cleanroom facilities. First, the trap chips were glued on a carrier PCB with a silver epoxy[4] or varnish[5]. The carrier PCB carrying the ion trap is made of Rogers 4350B material with copper metallization and galvanic gold coating. For electrical connectivity, the ion trap is wirebonded to the carrier PCB with gold wires of 25 µm thickness using a semi-automated bonding tool. The carrier PCB is then mounted on the copper holder with fork-shaped Titanium clamps. A further connection to the RF resonator PCB and DC filterboard is realized by additional wire bonds. This mounting procedure does not require the loosening of solder joints on the cryogenic electronics, when the ion trap is changed in the setup. Nevertheless, the whole assembly is inefficient regarding time and reliability, when many ion traps are to be tested. Therefore, an industrial assembly process was developed, performed at Infineon Technologies, as described in section 4.2.5.

[4]EPO-TEK® H20E-PFC

[5]Lake Shore Cryotronics, VGE-7031

4.4.3 Optical setup

To operate the ion trap experiment, in total six different lasers for photo-ionization, laser cooling and state manipulation of the trapped ions are required. This section describes the lasers provided for the experiment as well as the beam overlap achieved by the optical setup. More details are given in the master thesis of Regina Lechner [130] on the photoionization lasers, in the PhD thesis of Muir Kumph [131] on the cooling and repumping lasers, and in the master thesis of Roman Stricker [132] on the qubit laser.

Ionization

The calcium oven attached to the vacuum chamber generates single Ca atoms, which are ionized at the position of the trapping site. The ionization of the Ca atom is a two-step process: first, the atom is excited from the ground state 4^1S_0 to the first excited state 4^1P_1 with resonant laser light of 422 nm wavelength, which is provided by a 844 nm laser diode connected to a in-house cavity for frequency-doubling [130]. Second, the light from a 377 nm free-running laser diode is then used for the transition to the continuum.

Doppler cooling and detection

Doppler cooling and detection are performed using a laser with 397 nm wavelength, driving the transition from the ground state to the $4P_{1/2}$ state. Because there is a probability of around 6 % [51] for the excited state to decay into the $3D_{3/2}$ state, a 866 nm laser is used to repump the population back to the $4P_{1/2}$ state. To provide the 397 nm light, a diode laser of 794 nm wavelength is frequency-doubled and stabilized with a Fabry-Perot cavity locked via a Pound-Drever-Hall (PDH) lock [133]. By tuning the length of the cavity with a piezo-element, the frequency of the laser light is adapted. A similar locking scheme is also used for the 866 nm diode laser generating the light for repumping.

The optical transition from the $4P_{1/2}$ state to the ground state $4S_{1/2}$ is used for state detecting of the ion via fluorescence due to the short decay time of 10 ns [48] of the excited $4P_{1/2}$ state. Below the cryostat, a custom-made objective is placed to collect the emitted fluorescence photons from the ion. With a CCD camera, initial detection of a trapped ion as well as a first alignment of lasers and micromotion compensation are accomplished. Readout of the qubit state is realized by a photomultiplier tube (PMT).

Quadrupole transition

A laser at 729 nm drives the qubit transition $4P_{1/2} \rightarrow 3D_{5/2}$. The laser light is provided from a different laboratory in the same building. A Titanium-Sapphire laser stabilized

on a high-finesse cavity generates light with a bandwidth of only a few Hz. The light is then guided through a 200 m polarization-maintaining single-mode fiber to the Cryo-lab. Due to fiber noise, the linewidth increases to around 1 kHz after the fiber. For state initialization an additional laser of 854 nm wavelength is needed to shift the population via the $3D_{5/2} \rightarrow 4P_{3/2}$ transition down to the ground state. This laser is generated by a laser diode, which is stabilized with the PDH method similar to the lasers for Doppler cooling.

Beam overlap

For an easy alignment of the lasers on the ion, the 397 nm cooling laser, the 866 nm and 854 nm repumping lasers as well as the 422 nm and 377 nm photoionization lasers are overlapped outside the cryostat to enable a common position control with a single lens. The beam is aligned on the ion by moving the focusing lens mounted on a translation stage. The 729 nm qubit laser is entering the cryostat at 90° angle to the other lasers through another viewport. All lasers are in 45° angle to the quantization axis defined by the magnetic field. The laser setup is shown in figure 4.22.

Laser light sheet

The 2D twin trap is designed to trap multiple ions simultaneously. Because with the above described laser paths only one ion is addressed at the same time, a second laser path for the 397 nm and the 866 nm light is created, where the beam is spatially expanded to a laser light sheet. With two 30 mm cage systems the beams are independently shaped to an elliptical profile. Subsequently, they are combined to have one overlapping beam, which is focused and positioned on the ion trap by a spherical lens mounted on a translation stage. This beam path enters the cryostat at the side opposite to the original input of the cooling and photoionization lasers. The beam waist in direction perpendicular to the trap surface was measured to be $w_{0,y} = 10\,\mu\text{m}$ and $w_{0,y} = 25\,\mu\text{m}$ for the 397 nm and the 866 nm laser beams, respectively. In direction parallel to the trap, where the ions have a distance of a few 100 micrometer to their next neighbors, the beam waist can be tuned from $w_{0,x} = 150 - 1000\,\mu\text{m}$ for both lasers. A detailed description of the laser light sheet is given in [79].

4.4.4 Experiment control

The temperature of the cryostat, temperature sensors and an internal heater are controlled via a python program. There are two temperature sensors[6] placed at the

[6] LakeShore DT-670C-SD diode

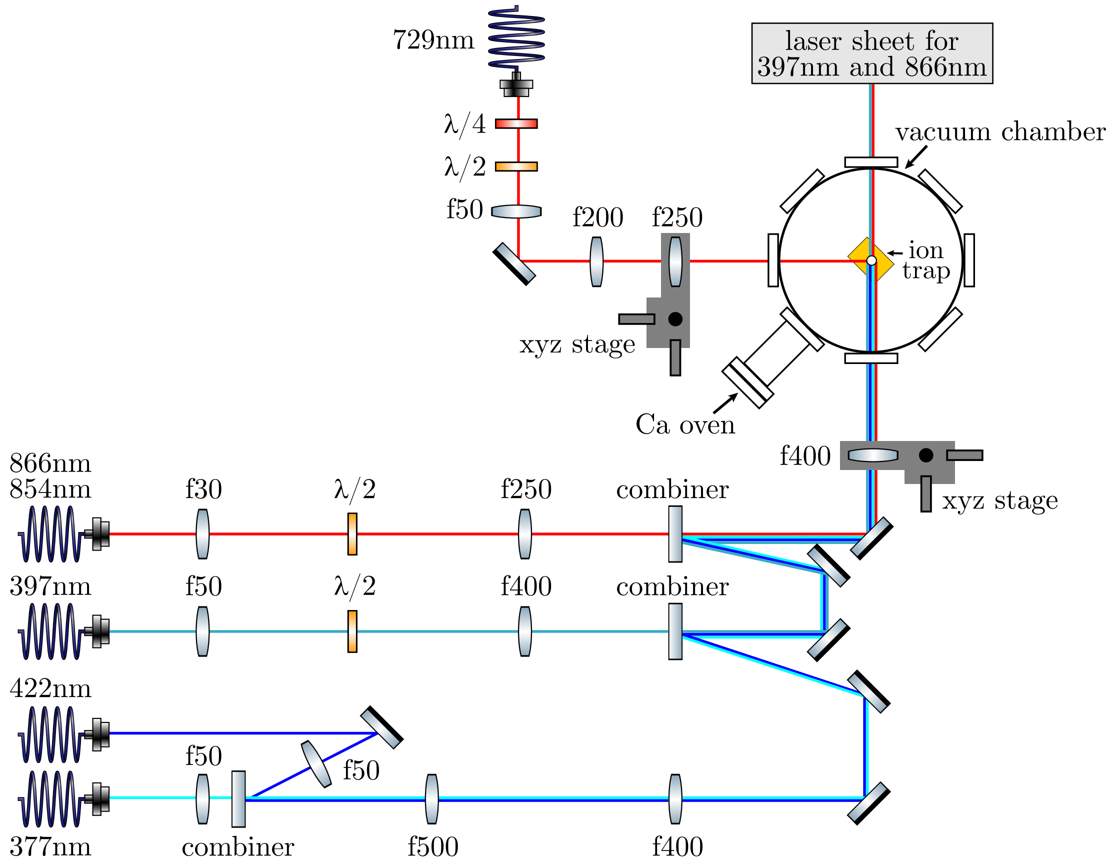

Figure 4.22: Schematic top view of the optical setup. Laser beams enter the cryostat on three sides through viewports and reach the ion in 45° angle with respect to the trap axis. The photoionization lasers with 422 nm and 377 nm wavelength are overlapped with the 397 nm cooling laser and both repumping lasers (866 nm and 854 nm) by combiners and are jointly controlled by a focusing lens mounted on a xyz translation stage. The qubit laser beam (729 nm) enters the cryostat in 90° angle to the other lasers. A laser light sheet (viewport opposite the overlapped beam) for the 397 nm and 866 nm lasers allows for addressing multiple ions simultaneously.

50 K and 10 K shield, respectively. The temperature is measured and stored in influxDB, where the set points for the internal heater are set. Additionally, the vacuum pressure gauge is logged in this way. A Grafana [134] interface serves as a graphical visualization dashboard allowing for simple readout of temperatures and pressure.

Optics and electronics are controlled via a LabView program called QFP 2.0, specially designed for the ion trap experiments at the University of Innsbruck. This program controls acousto-optical modulators (AOMs) of the 397 nm, the 866 nm and the 854 nm

laser beams and tracks fluorescence counts on the PMT for state readout. The same LabView program also controls the pulse sequencer box (pulse box) used to generate RF signal pulses and digital outputs [135]. In this way, the 397 nm, the 866 nm and the 854 nm laser beams are switched on and off. With the RF pulses, the AOM of the 729 nm is controlled to generate pulse sequences of various amplitude, frequency, duration and phase. The RF voltage applied to the trap's RF electrodes is generated by a function generator[7]. A low-noise voltage source[8] creates the DC voltages for the DC trap electrodes. These voltages are reduced with a factor of 10 by a voltage devider, to adjust the voltage more precisely before applied to the trap electrodes.

4.5 Ion trap performance

Ion traps of the design with 120 µm ion-surface distance were characterized in the so called cryolab experiment at the University of Innsbruck, using the cryogenic setup described in section 4.4. Several iterations of ion traps, substrate materials and adapted layout were investigated and are presented in the following.

4.5.1 Substrate influence on the RF resonator

To generate the required RF voltage of 180 V for loading ions, a step-up resonator as described in section 4.4.2 was used. For an optimized matching of the resonator circuit at cryogenic temperatures, the quality factor Q of the resonator was measured dependent on the temperature to determine the RF voltage gain. The quality factor changes with temperature, because charge carriers in the substrate freeze out if the trap reaches temperatures lower Than the transition temperature of around 30 K. This leads to a reduction of the trap capacitance, changing the resonance frequency and thus the quality factor of the resonator. The measured data is shown in figure 4.23a. Only for temperatures below 25 K the Q factor reaches values > 100. For the used setup, a voltage gain > 30 is required to provide the RF voltage of 180 V for stable trap operation.

To determine the temperature of the ion trap and thus the Q factor of the resonator during trap operation, the measured resonance frequency is compared to data taken for a full cool-down without applied RF voltage. The quality factor and temperature measured at this resonance frequency suggests the trap temperature during operation. Following this method, a trap temperature of 50 K was estimated when applying an RF voltage of 180 V. We suspect heating of the trap chip due to Ohmic losses in the

[7]Marconi instruments 2024
[8]ISEG, EHS F205x-F-K1

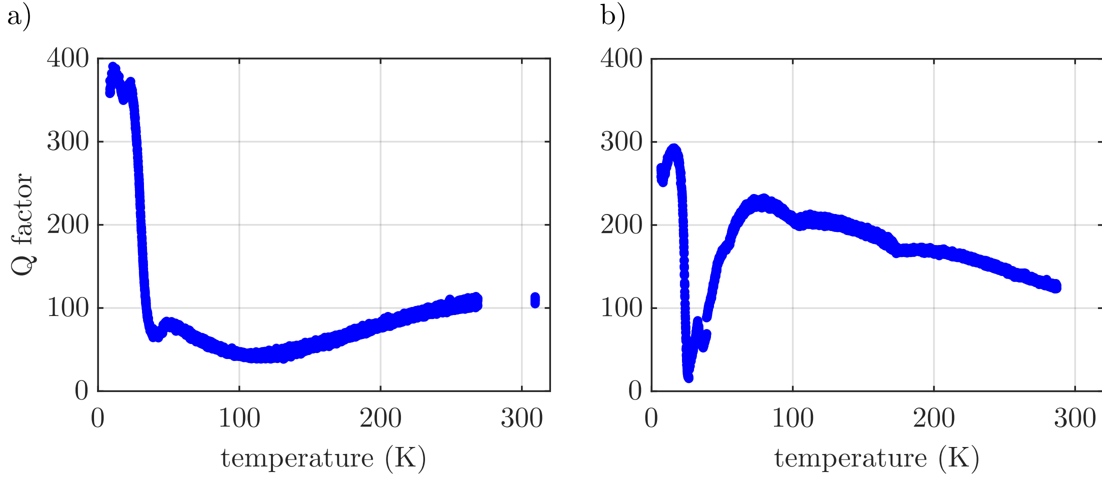

Figure 4.23: Q factor of the resonator dependent on the temperature of the ion trap. a) Ion trap on a standard silicon substrate with 3 Ω cm resistivity. Q-factors > 100 are only found at temperatures $T < 25\,\mathrm{K}$, which defines the temperature limit for stable trap operation via the obtainable step-up voltage. b) Ion trap on a silicon substrate with $\rho > 8\,\mathrm{k\Omega\,cm}$ resistivity. A significant drop of the Q factor between $25 - 50\,\mathrm{K}$ is visible. Error bars are smaller than the displayed measuring points.

substrate in the area of the bond pads, which is not shielded by the metal 1 ground plane. To achieve the required RF amplitude on trap despite the low Q factor of $Q = 80$ at this temperature, even higher RF voltages need to be applied, resulting in a further heating of the trap.

One approach to solve this issue is using a high-Ohmic substrate to reduce heating of the trap during operation, as with a higher resistivity the loss tangent of the material decreases, see section 4.2.1. Therefore, an ion trap with a high-Ohmic substrate with $\rho > 8\,\mathrm{k\Omega\,cm}$ resistivity was fabricated and characterized in the experiment. The measured Q factor dependent on trap temperature for this substrate is shown in figure 4.23b. As expected, the quality factor at room temperature for the high-Ohmic substrate with $Q \approx 130$ is higher than for the standard substrate with a higher loss tangent, which only reaches a factor of $Q \approx 100$. The Q factor for the high-Ohmic substrate increases with decreasing trap temperature due to the matching of the RF resonator, but a drop between $25 - 50\,\mathrm{K}$ was observed, reaching a minimum value of 15. This behavior can be explained by light-induced charges in the unshielded substrate area, generated by the room light in the laboratory that was not turned off during the measurement. These photo-generated charges increase the capacitance between RF and substrate due to a parasitic MOS capacitor created between the RF electrodes and the substrate, as

discussed in section 4.3.3. An increased trap capacitance together with a change of the dielectric loss tangent leads to a shifted resonance frequency and thus a reduction of the resonator's Q factor in the unmatched circuit. Since silicon has a low band gap of 1.17 eV at temperatures of $T = 10\,\mathrm{K}$ [136], all lasers used in the experiment have a sufficiently high energy to generate charge carriers in the substrate during trap operation [124]. For this reason, operation of the trap in a dark environment without room light will also lead to light-induced charge carriers and the observed behavior cannot be avoided.

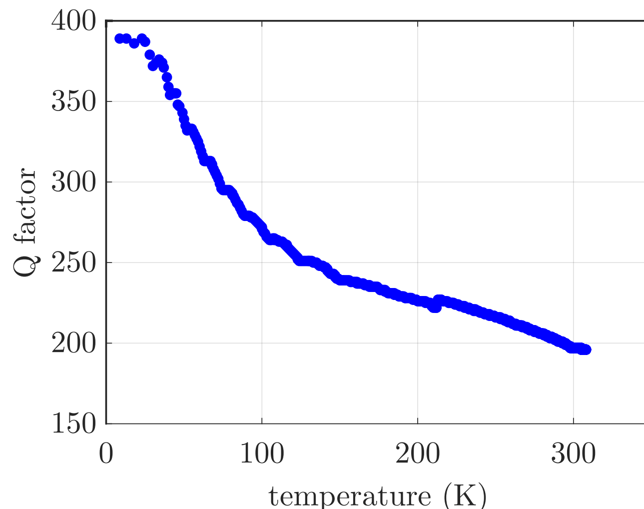

Figure 4.24: Q factor of the resonator dependent on the temperature for the twin trap 2.0 in which the substrate is shielded along the entire chip area. The Q-factor is a monotonous function of the substrate temperature as expected for an ion trap representing an ideal capacitor. Q-factors ~ 390 are obtained at temperatures $T < 25\,\mathrm{K}$, enabling a high voltage gain as required for stable ion trap operation. Error bars are smaller than the displayed measuring points.

Since the RF resonator performance is limited for both the standard and the high-Ohmic silicon substrate, the layout of the ion trap was changed to extend the substrate shielding in the metal 1 layer also to the bond pad area, as shown in figure 4.25. This redesign is referred to as twin trap 2.0. The Q factor of the 2D twin trap with standard silicon substrate and full-area shielding layer is not affected by Ohmic losses, as visible in figure 4.24. Therefore, a sufficient voltage gain ≈ 33 of the step-up resonator is achieved to provide the 180 V RF voltage needed for trap operation without significant heating of the ion trap.

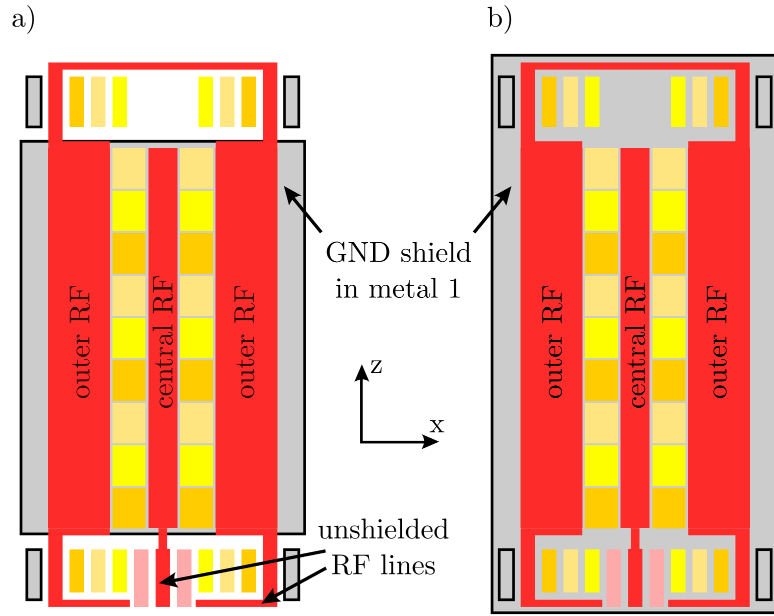

Figure 4.25: Schematic of the trap layout with RF electrodes (red), DC electrodes (shades of yellow) and a GND shield in the metal 1 layer (gray). a) In the original design, the GND shield in the metal 1 layer does not extend to the bond pads, thus there are unshielded RF lines in the bond pad area. b) In the twin trap 2.0 the GND shield extends to the chip edge, shielding the RF lines also in the area of the bond pads.

4.5.2 Ions trapped in two arrays

For the first loading attempts in the 2D twin trap, only one RF resonator was used to reduce the complexity of the setup. Thus, on all three RF rails the same RF voltage of 180 V at a drive frequency of 25 MHz was applied. The ion trap hosts in total 78 electrodes. Because there are only 20 connection lines routed out of the cryostat to the DC supply, multiple electrodes are combined on the carrier PCB: electrodes in the central interaction zone are merged with the corresponding periodically connected DC island electrodes. This results in two independent parallel 1D arrays separated by the central RF rail, similar to the configuration depicted in figure 4.4a. Thus, only four different DC voltages for each 1D array are needed for operating the ion trap. The voltage amplitudes are in the range of ± 10 V.

After successfully trapping single ions in different trapping sites, the laser sheet as described in section 4.4.3 was introduced to trap ions in multiple trapping sites simultaneously. The laser sheet has a beam waist of up to $w_{0,x} = 1000\,\mu\text{m}$ in parallel to the trap surface. Thus, up to six neighboring trapping sites in both arrays can be

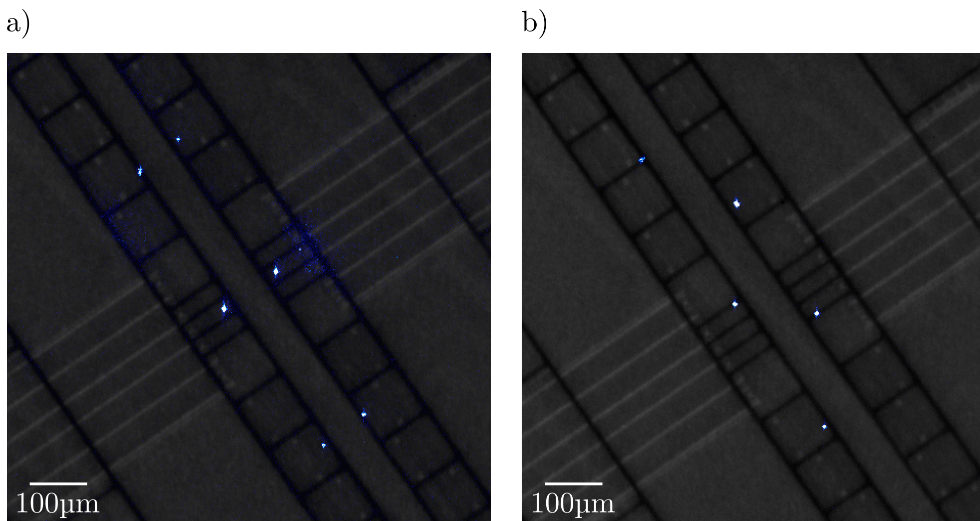

Figure 4.26: Ions (white dots) trapped in a a) rectangular and b) triangular configuration in the 2D twin trap. The ion trap layout with segmented electrodes is visible in gray. Figure adopted from [29].

reached by the cooling and repumping laser. To load ions in different trapping sites, two techniques were employed: either the photo-ionization laser beam was focussed on the desired lattice site, or the ion was trapped in the central trapping zone and shuttled to the desired position by tuning the voltages applied to the segmented DC electrodes. The latter technique was introduced, because in some trapping sites no ions could be successfully loaded. In figure 4.26, two microscopic images showing a rectangular and a triangular trapping configuration with six and five ions, respectively, are depicted. The triangular configuration was achieved by shifting the ions in both 1D arrays by each a quarter lattice period in opposite direction. Ion shuttling in an ion trap array is an important method for quantum information processing, as it allows for entanglement between non-nearest neighbors in the array, as described in section 4.1.

4.5.3 RF induced magnetic fields

During trap characterization, a drift of the carrier transitions from the $4S_{1/2}$ to the $3D_{5/2}$ manifold ($\Delta n = 0$) was observed. To further investigate this behavior, the carrier transitions were recorded while changing the RF power applied to the trap's RF electrodes and for a constant external magnetic field. In figure 4.27 the data showing the frequency shift dependent on the RF power for different transitions is depicted.

Although this behavior is not fully understood at this point, we suspect a parasitic magnetic field induced by the trap's RF electrodes, resulting in an AC Zeeman shift.

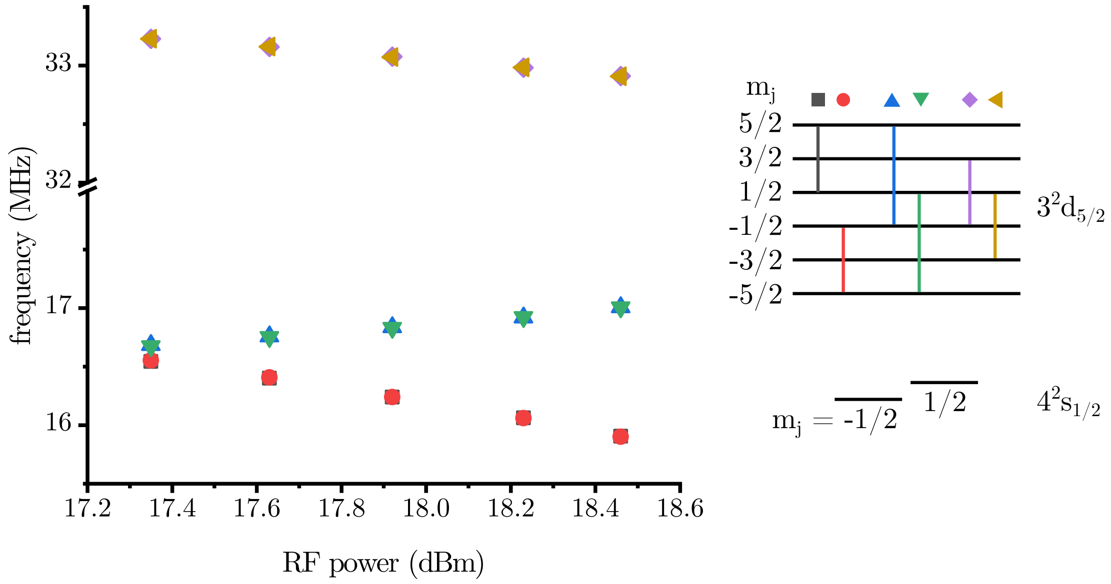

Figure 4.27: Transition frequencies dependent on the RF power. Every data point represents the frequency difference between two transitions, as depicted on the right side. A shift in the transition frequencies with changing RF power of all transitions is clearly visible.

The capacitance of the RF electrode to the GND electrode in the metal 1 layer (see 4.3.3) combined with the applied RF voltage of 180 V creates a time-varying charging of the RF electrodes with the RF frequency. This results in an oscillating current on the RF electrodes and hence an oscillating magnetic field. All three RF rails are connected to the same RF resonator by wire bonding to the same lead at the carrier PCB. Here, the outer RF electrodes are wire bonded from one bond pad, while they are connected on the opposite side of the trap chip, as depicted in figure 4.28. Due to the relatively high RF capacitance, this leads to a non-negligible oscillating current flowing in two opposing directions in the area of the trapping sites. If this magnetic field is not negligible with respect to the external magnetic field, it changes the bias B-field and can affect the quantization axis and thus the frequencies of the carrier transitions in the trap.

To solve this issue, the connection between the outer RF electrodes was cut in the twin trap 2.0 redesign. Moreover, bond pads for both electrodes were integrated to simplify wirebonding to the same lead on the carrier PCB, as shown in figure 4.29. A measurement of the transition frequencies in the twin trap 2.0 is shown in figure 4.30. We want to emphasize, that no AC Zeeman shift and therefore no change in transition frequencies was observed.

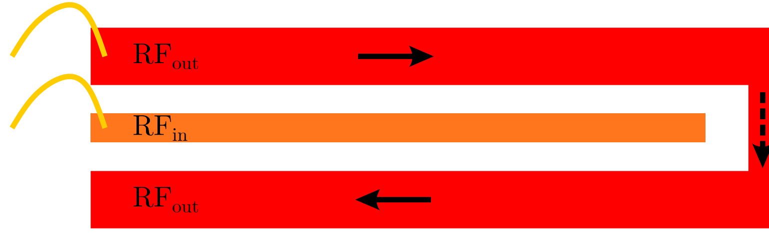

Figure 4.28: Schematic of the electric connection of the RF electrodes. The two outer RF electrodes RF_{out} (red) are wire bonded (yellow) from only one bond pad, while they are connected on the opposite side of the trap chip. This causes an opposing direction of the current flow in these electrodes in the area below trapped ions.

4.5.4 Heating rate measurements

To evaluate the ion trap performance related to possible quantum operations, heating rate measurements of the 2D twin trap were performed for different trapping sites. Values between around (100-500) q/s were measured for different trapping sites around the trap center and axial frequencies of $w_z = 2\pi \times (1.2 - 1.5)\,\mathrm{MHz}$. Possible reasons for the relatively high heating rate are surface noise due to native oxide on the AlSiCu electrodes [137] and the gap oxide (see section 3.2.1), or technical noise. Another hypothesis is adsorbates on the trap surface [138] such as a contamination with Calcium atoms sticking to the AlSiCu electrodes.

To reduce the influence of suspected surface noise due to possible contaminations and native oxide on the trap surface, the fabrication routine was adapted as described in section 4.2.3. After structuring the metal 3 layer, another isotropic etch process was introduced to remove the oxide in the gaps between the electrodes. Moreover, the whole wafer surface was coated with gold. Since gold does not form a native oxide, the effects of stray charges on the metal surface can be reduced. The best heating rate of a 2D twin trap with these improvements and with an axial frequency of $w_z = 2\pi \times 1.2\,\mathrm{MHz}$ shows a value of 33(10) q/s, determined by driving Rabi oscillations on the blue sideband (see section 3.2.2). A plot of the mean phonon number dependent on the wait time is shown in figure 4.31. Due to the large uncertainty, this result is only meaningful to a limited extent. Nevertheless, it suggests an improvement of around one order of magnitude compared to the heating rates measured in the original trap. This ion trap was not investigated further as the fabrication of the new ion trap with improved layout was completed and it was incorporated into the experiment.

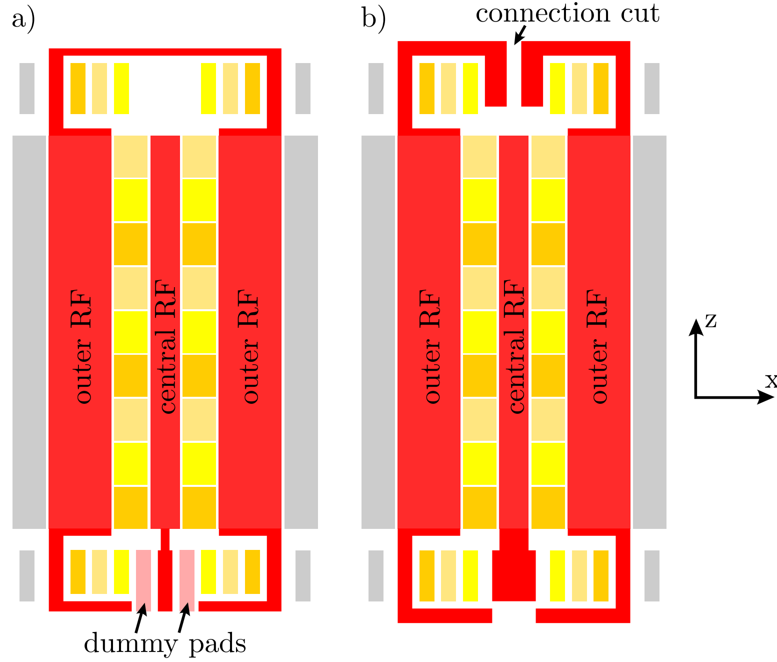

Figure 4.29: Schematic of the trap layout with RF electrodes (red), DC electrodes (shades of yellow) and GND (gray). a) In the original design, the two outer RF rails are connected on one side of the trap chip. Dummy bond pads without connection to electrodes are located next to the central RF bond pad. b) In the twin trap 2.0 the connection line between the two outer RF rails is cut and bond pads are integrated to simplify wirebonding to the same lead on the carrier PCB. The dummy pads are removed to enlarge the central RF bond pad.

4.5.5 Discussion and outlook

We realized the concept of a two-dimensional ion trap array, capable of trapping ions in two linear strings of individual trapping sites. The successfully microfabricated ion traps were electrically characterized before the performance in the ion trap experiment was tested. Simultaneous trapping of up to six ions in a two-dimensional multi-well was achieved. Three main observations were found and presented in this thesis:

- **Influence of the silicon substrate on the RF resonator** If the traps's silicon substrate is not shielded, high RF losses lead to heating and a decreased voltage gain of the RF resonator. This issue occurred for both a standard silicon substrate and a high-Ohmic silicon substrate. The twin trap 2.0 redesign with full-area shielding solved this issue. Nevertheless, a change to substrate materials with low loss tangent and large band gap such as fused silica ($E_g = 7 - 9\,\text{eV}$,

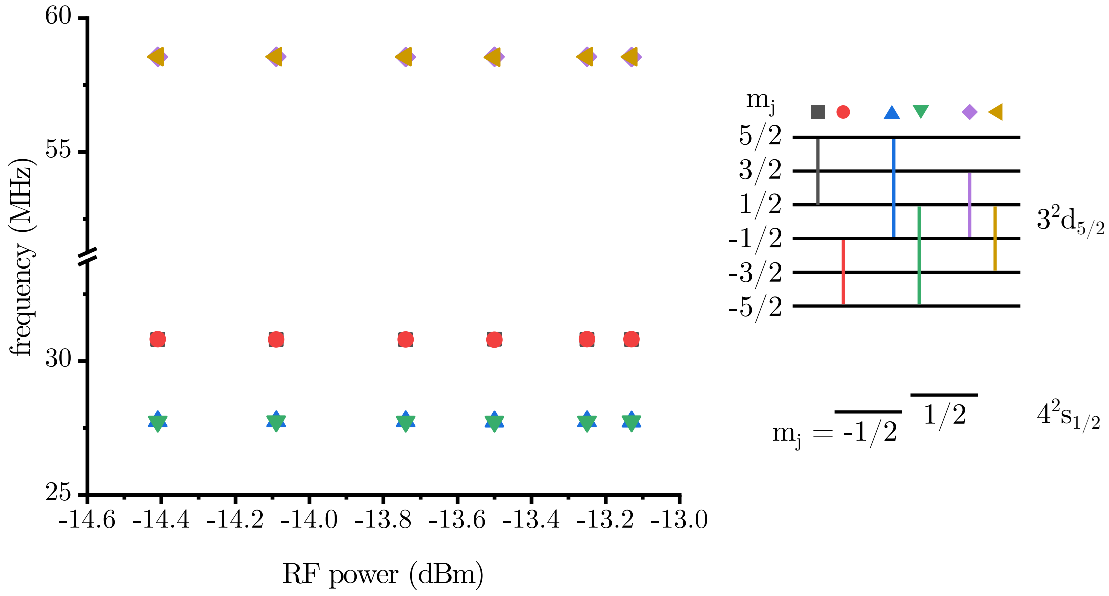

Figure 4.30: Transition frequencies dependent on the RF power after changing the wiring of the RF electrodes. No dependence of the transition frequencies on the RF power and thus AC Zeeman effect is visible.

$\tan(\delta) \sim 10^{-4}$)[139] or sapphire ($E_g = 8.5\,\mathrm{eV}$, $\tan(\delta) \sim 10^{-4}$)[140] is desirable to further minimize negative influences of the substrate to the ion trap performance. Moreover, with a wide-bandgap substrate material there is no need for a shield layer, thus the trap capacitance is significantly reduced.

- **AC Zeeman shift caused by RF wiring** An AC Zeeman shift of the carrier transitions was observed in the 2D twin trap, caused by an oscillating magnetic field. The relatively high RF capacitance of the ion trap leads to an oscillating current on the RF electrodes, resulting in a time-varying magnetic field. A connection of the outer RF electrodes on one side of the trap chip led to an opposing direction of the current flow at the position of the ion. With the twin trap 2.0 redesign, the issue of shifted transition frequencies was solved. Moreover, a reduction of the trap capacitance helps to avoid undesired magnetic fields induced by the RF electrodes. Using a substrate material as fused silica obviates the need for a shield layer, therefore enabling a significant reduction of the RF capacitance.

- **Heating rates** In the first characterized 2D twin trap heating rates in the range of (100-500) q/s for different trapping sites were measured. Explanations for this relatively high heating rate are either a surface contamination, exposed gap oxide or native oxide on the AlSiCu electrodes. Adding a gold coating of the

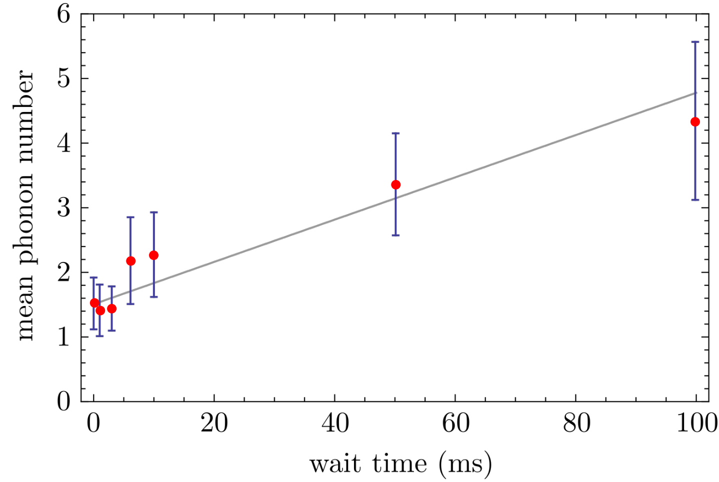

Figure 4.31: Heating rate measurement of the 2D twin trap with gold surface and underetched electrodes, determined by driven Rabi oscillations on the blue sideband. The mean phonon number is measured dependent on the waiting time. A linear fit to the data (gray solid line) reveals a heating rate of of 33(10) q/s.

trap electrodes and decreasing the amount of exposed gap oxide revealed a lower heating rate of 33(10) q/s. Therefore, non-oxidizing electrode materials, shielding of dielectrics and an in-situ cleaning of the ion trap inside the cryostat should be considered to improve the ion trap performance in future iterations.

To create a two-dimensional array of entangled ions in the 2D twin trap, the inter-ion distance needs to be reduced to increase the coupling rate. Shuttling of ions along the linear array (parallel to the trap axis) was successfully performed as described in [29]. To couple ions along the radial multi-well created by the RF electrodes, the central and outer RF electrodes need to be driven independently. By reducing the amplitude of the central RF rail, the distance between the ions decreases. Since the RF voltage is amplified inside the cryostat, a second RF resonator was fabricated and integrated into the setup, as shown in figure 4.32.

This resonator is similar to the first one, but has an additional adjustable capacitor, to allow for tuning the resonance frequency. For the experiment, it is crucial that both resonators are matched in resonance frequency and phase. If one of the two mentioned properties are shifted in one resonator, no RF null is present in the trap. This leads to micromotion that cannot be compensated [79]. A detailed description of the characterization of the second resonator and the new trap setup is subject of Marco Valentini's PhD thesis. By coupling ions in both lattice directions, entangled qubits

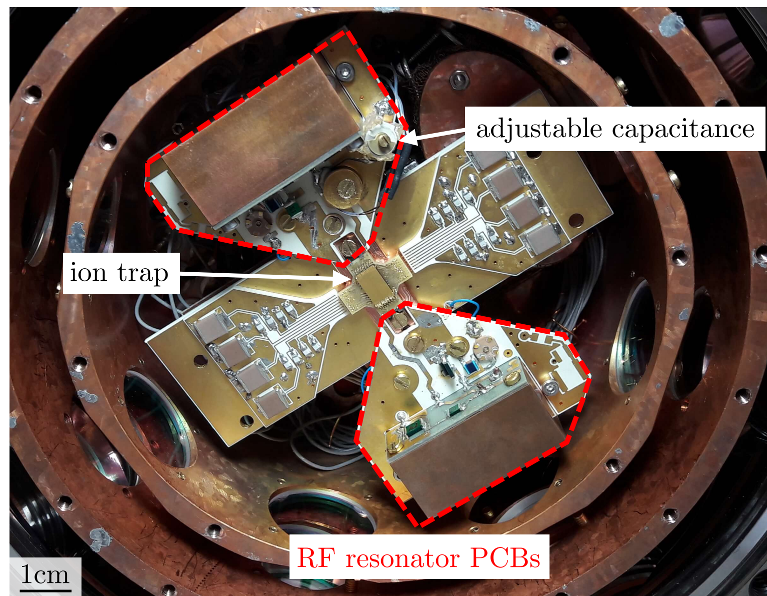

Figure 4.32: Trap setup with two RF resonators (red). An adjustable capacitance allows for tuning the resonance frequency of the second resonator to match the one of the first resonator. This is needed to achieve a sufficient enhancement of the RF amplitude for both RF electrodes.

for quantum information processing are created. If efficient coupling in this proof-of-principle experiment is shown, an important step towards a large-scale trapped-ion quantum computer is made.

Chapter 5

3D MEMS ion trap

The contents of this chapter are also included in the Patent submitted to the EPA with official application file reference 21185020.1 on 12th July 2021.

An article has been published with the title "Industrially microfabricated ion trap with 1eV trap depth", S. Auchter et al., Quantum Science and Technology (2022) [141].

The trap concept was developed by researchers at ETH and the University of Innsbruck, including the author. Simulations were conducted by the author and Marco Valentini. Fabrication and quality analysis of the ion trap were carried out by the author. The trap characterization was performed by Chiara Decaroli and Chris Axline at ETH.

Microfabricated planar ion traps represent an important step towards a scalable quantum processor, enabling complex trap layouts on small chips with individual control of single ions. However, due to the weak confinement potential of around 100 meV [68, 102, 142], such traps show limitations with regard to operation temperature, speed and reliability of ion shuttling within the trap [19, 85] as well as ion storage times [33], as described in detail in chapter 3.

In the PIEDMONS project (Portable Ion-Entangling Devices for Mobile-Oriented Next-generation Semiconductor-Technologies) [143], researchers from the University of Innsbruck, ETH Zurich and Infineon Technologies are developing scalable, microstructured ion traps with an enhanced confinement potential. Within the project, an ion trap with a trap depth of 1 eV [141] is realized based on micro-electro-mechanical systems (MEMS) fabrication technologies. An industrial microfabrication of the ion trap allows for a reliable production of identical devices due to automated and strictly controlled processing. Furthermore, it supports integration of optics [38, 39] and electronics [36,

37].

This chapter presents a hybrid ion trap, consisting of a surface trap above which additional DC electrodes are wafer-bonded to enhance the depth of the confinement potential. This trap combines the advantages of planar ion traps enabling complex, scalable layouts possible through microfabrication, and three-dimensional linear ion traps featuring a deep confinement potential. The hybrid ion trap is called 'Azkaban', named after the prison from which not even witches and wizards can escape [144]. In the following, the design of the hybrid trap is described in detail, and an overview on the fabrication process, quality analysis and a characterization of the ion trapping performance is given.

5.1 Trap design

In this section the design of the hybrid ion trap is presented. This includes simulations to find the optimal trap geometry and corresponding trapping parameters. Moreover, the routing and layer stack forming the ion trap as well as the design rules for the layout that must be adhered to for a successful trap fabrication are described.

5.1.1 Trap concept

To realize the vision of a microstructured ion trap with deep confinement potential, many different concepts have been developed and discussed regarding fabrication possibilities and requirements of the ion trap experiment.

The concept that was chosen consists of a surface trap as a bottom layer extended by additional electrodes on a top layer to enhance the trap's confinement potential, as shown in figure 5.1. The bottom and top layer are separated by a spacer to create the topology of a 3D trap architecture. This ion trap fulfils the criterion of scalability in terms of i) number of trapped ions by using a scalable, planar ion trap layout with microstructured, segmented electrodes, and ii) design complexity by including additional functionality such as junctions or dedicated trap zones.

The bottom layer is formed by a silicon substrate with metallic electrodes that are routed using multiple metal layers. Therefore, a simple version of the 2D ion trap layout, as presented in section 4, with just one trapping zone is used. The spacer is defined by a 400 µm thick glass wafer, which sets the ion-surface distance to the top and bottom electrodes to around 200 µm. In the presented prototype, the spacer does not carry additional functionality like for example optical or electrical connections. For the top layer, doped silicon is chosen as the conductive material forming the electrodes. This wafer is then anodically wafer-bonded to the glass spacer.

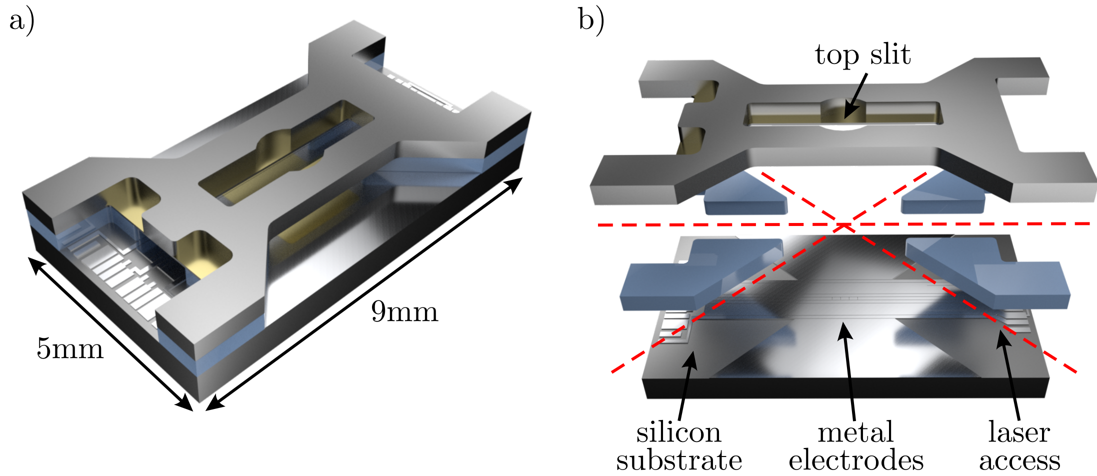

Figure 5.1: Rendering of the hybrid ion trap consisting of three layers in a) assembled view and b) explosion view. Metallic electrodes (bright gray) on a silicon substrate (dark gray) form the bottom electrodes. A glass spacer (blue) defines the distance between bottom and top electrodes. Openings in all lateral directions allow for laser access (red lines). Two electrodes on the top layer made of highly doped silicon coated with gold (gold) are placed in parallel to the trap axis. A slit in the top layer allows for fluorescence detection.

An important challenge of the 3D architecture is to provide high optical access to allow for laser cooling and manipulation parallel to the trap surface as well as state discrimination by fluorescence detection from top. Therefore, holes are necessary in the spacer so that laser light approaches the trapped ion in a 45° angle relative to the trap axis to enable laser cooling of all motional modes, see section 2.4. Moreover, the top layer is recessed in the area above the trap center, where the ion is trapped and fluorescence photons are collected.

The dielectric glass spacer and silicon surfaces should be placed as far as possible from the ion to reduce the effects of stray charges, if shielding is not possible. Stray charges and surface electric field noise might push the ion out of the RF null and thus increase micromotion [145]. To address this possible issue the glass spacer has a distance >1.5 mm to the simulated trapping position, reducing the effects of stray electric fields, which depend strongly on the ion-surface distance d with $S_E \propto \frac{1}{d^3}$. For the same reason, the silicon substrate of the top wafer is recessed around the slit to reduce the amount of exposed silicon. The doped silicon forming the electrodes on the top wafer is coated with a thin gold layer, since there is a lack of experience on the compatibility of doped silicon as electrode material in ion traps [99].

Using a glass wafer as spacer has the advantage of enabling an anodic bonding process

to connect the three wafers. Anodic bonding is well established at the Infineon fabrication facility, being considered reliable and robust with respect to surface roughness.

5.1.2 Geometry and simulations

To optimize the geometry of the ion trap in terms of trap depth and stability of the trapped ion, finite-element method (FEM) simulations using COMSOL Multiphysics were carried out. The simulated electric fields are exported and analyzed with the COMSOL to MATLAB Livelink. In the following section the geometry of bottom and top electrodes, as well as the simulated confinement potential and trap parameters are described. A detailed simulation analysis including the description of the used algorithms will be provided in Marco Valentini's PhD thesis [111].

The following requirements to the ion trap geometry were identified:

- **Confinement potential**: A deep confinement potential of ~1 eV should be achieved to allow for longer ion-lifetimes compared to standard surface traps.
- **NA**: A state-of-the-art numerical aperture (NA) for fluorescence detection of at least 0.7 is targeted to enable reliable readout of the ions' state when performing quantum operations.
- **Secular frequencies**: Radial motional frequencies of at least 1.5 MHz and an axial motional frequency of 1 MHz are typically used to realize stable trapping of ions.
- **Micromotion compensation**: Suitable DC shim sets for compensation of micromotion are necessary to achieve low heating rates forming a reliable basis for quantum information processing.
- **Laser cooling**: A sufficient tilt of the radial oscillation axes with angles $\geq 10°$ is required to enable laser cooling with one laser beam parallel to the trap surface.
- **RF frequency**: The applied RF trap frequency should be in the range of (20-50) MHz for stable trapping of ions in the quadrupole potential generated by the RF electrodes.
- **DC voltages**: To reduce heating of the trap chip and avoid damage due to breakdown between electrodes or narrow leads, the DC voltage amplitudes should not exceed 25 V.
- **q-factor**: To guarantee stable trapping, the stability q-factor of the ion trap should be ≤ 0.4.

- **Single ion addressing**: In order to allow for reliable single or multi qubit gates, independent addressing of single trapped ions must be ensured.

Geometry of the bottom electrodes

The bottom layer of the hybrid trap forms a surface trap with two RF electrodes surrounded by DC electrodes, confining the ion in the radial direction. A segmentation of the central DC rail enables axial confinement of the ion in the trap. In order to find a suitable geometry that supports the target concept, FEM simulations were carried out, adapting the size and position of several electrodes. In figure 5.2 the geometry of the bottom electrodes is depicted: two 400 µm wide RF rails are located on both sides of three central DC electrodes. Here, a segmentation of the innermost DC electrode in five segments along the trap axis is used to create confinement in axial direction. The central three ’island’ electrodes have a length of 200 µm. This segmentation also allows for moving the ion a few 100 micrometers along the trap axis. Because a distance of 300 µm in between the two RF electrodes is needed to achieve the targeted ion-surface distance of 200 µm, DC compensation electrodes are placed next to the central DC rail. These DC electrodes are necessary for micromotion compensation and to provide a tilt of the radial modes. All three DC rails have a width of 100 µm. On the outer sides of the RF electrodes, additional DC compensation electrodes are positioned, which extend to the chip edge in the area that is not bonded to the spacer. These electrodes shield the underlying silicon substrate. Gaps between RF and DC electrodes have a width of 9 µm, gaps between DC segments are 5 µm wide. All electrode dimensions are also listed in table 5.1.

Table 5.1: Width and length of bottom and top electrodes of the hybrid trap.

electrode	width along x (mm)	length along z (mm)
A	0.1	0.2
B1/B2	0.1	0.2
C1/C2	0.1	3.2
1	0.1	> 7
2	0.077 / 1.8	> 7
RF	0.4	> 7
top	1	6.6

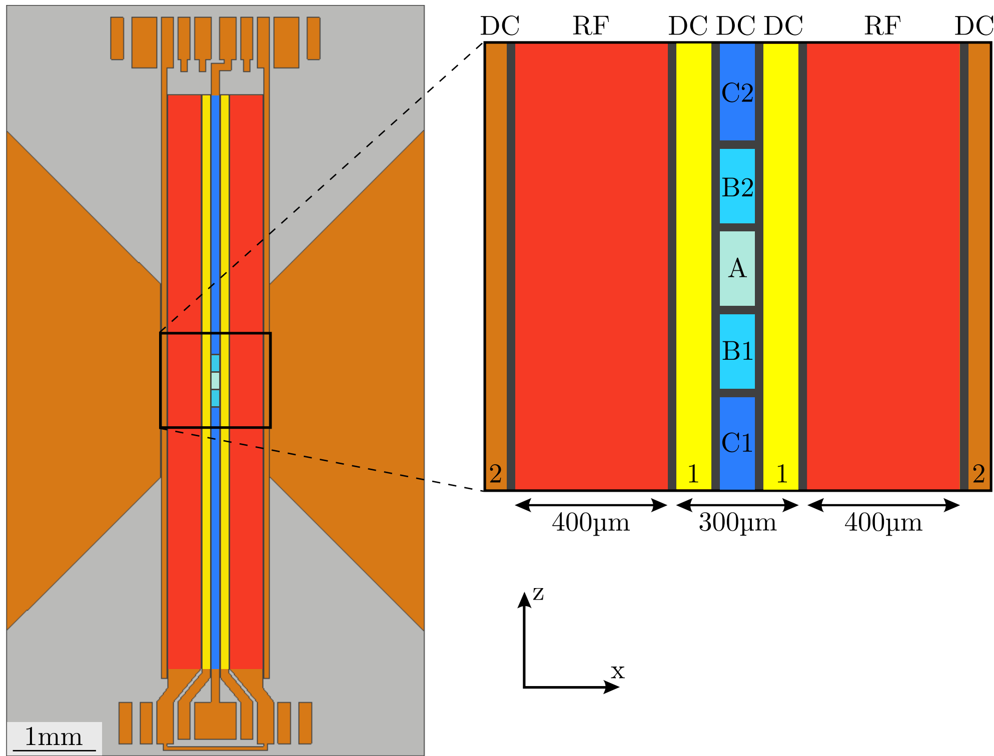

Figure 5.2: Geometry of the hybrid trap bottom layer. Two parallel RF rails (red) are surrounded by DC electrodes (yellow and orange, marked as 1 and 2) used for micromotion compensation. In the trap center, segmented DC "island" electrodes (shades of blue, marked as C2, B2, A, B1, C1) create the confinement in axial direction.

Geometry of the top electrodes

To enhance the confinement potential, two additional top electrodes are integrated 400 µm above the surface trap. In the ion trap prototype, two DC electrodes are implemented, parallel to the trap axis. In future designs, this number can be scaled and extended to RF voltages, dependent on the desired trap geometry. Optical access is ensured by a slit between the top electrodes. The width of this slit affects both trap depth and the ion-surface distance, since the position of the electrodes influences the direction of electric field lines in the trap. Therefore, the slit width as well as the top electrode width was varied in a simulation to find an appropriate dimension of the top electrodes that still facilitates a state-of-the-art NA of ≥ 0.7 [146, 147] to collect photons for state detection. In figure 5.3, the simulated RF trap depth and NA dependent on the slit width between the top electrodes for an RF voltage of $V_{\mathrm{RF}} = 200\,\mathrm{V}$ is depicted. We chose the 1 mm wide top electrodes to be separated by a slit of 550 µm width. This

results in an NA of 0.75 and a confinement potential of 295 meV without additional DC bias at an ion-surface distance of ∼200 µm. When estimating the optical access from top, also the substrate silicon of the top wafer needs to be taken into account. Here, the silicon is recessed on both sides of the slit by 200 µm with an additional circular recess at the position above the central trapping site, as visible in figure 5.4. Two trap versions with different amount of recess are designed. A recess of 400 µm provides an NA of 0.72, a recess of 700 µm provides an NA of 0.83 (neglecting the slit between the top electrodes, which results in an NA of 0.75). The two trap versions are referred to as SI-400 and SI-700, respectively.

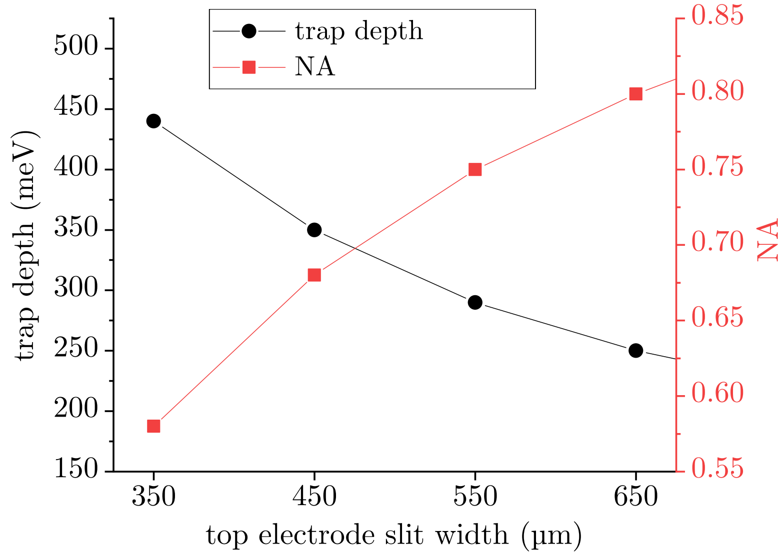

Figure 5.3: Trap depth (black circles) and NA for fluorescence detection (red squares) dependent on the width of the slit between the two top electrodes.

Finally, the mechanical stability of the free-standing top electrodes was simulated with FEM simulations in COMSOL. Undesired mechanical resonances of the electrodes at the trap drive frequency may lead to vibrations, modulating the electric field and noise. The first 50 modes of mechanical vibration are found at frequencies in the range of (0.2 - 2.0) MHz. At typical RF drive frequencies around (15-50) MHz, no eigenvalues are found. Thus, there are no natural frequencies in this frequency range.

Trap depth

Another target of the simulation study is to investigate the improvement of trap depth in the hybrid trap compared to a planar surface trap. Figure 5.5 depicts the pseudopotential for an RF voltage of $V_{\mathrm{RF}} = 200\,\mathrm{V}$ of the simulated hybrid trap and a surface trap without top DC electrodes as a reference. The pseudopotential is a useful tool in ion

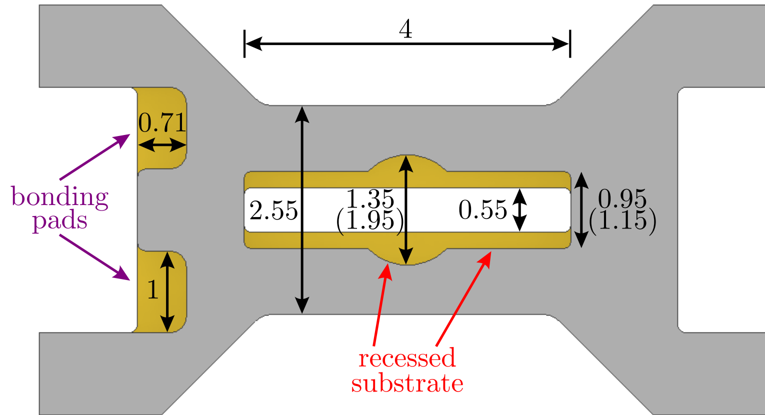

Figure 5.4: Sketch of the top layer dimensions, with units given in millimeter. Conductive silicon visible from top is colored yellow, substrate silicon is colored gray. The top electrodes have a width of 1 mm.

trap simulations, as it describes the confinement of the ion in the trap in all spatial directions. For the comparison the geometry of the surface trap was scaled down to achieve the same ion-electrode distance of 200 µm as the hybrid trap, which is achieved with an electrode width of each 100 µm for a DC electrode in the center of two RF electrodes. With the top electrodes set to ground, already a clear improvement in trap depth is visible. The confinement potential can be further enhanced by adding DC voltages on the various DC electrodes. With the voltage set given in table 5.2, a trap depth exceeding 1 eV is achieved, as shown in figure 5.6.

Voltage set for trap operation

In the first iteration of ion traps the two top DC electrodes were electrically shorted (see section 5.3.4). Due to the constrained flexibility of applied voltages, the achievable trap depth was limited if a sufficient tilt of the radial mode axes for laser cooling was provided at the same time. A DC voltage set optimized for a deep confinement potential is given in table 5.2. With an RF voltage of $V_{\mathrm{RF}} = 183\,\mathrm{V}$ at a trap frequency of 20.6 MHz, a trap depth of $V_{\mathrm{dc,3D}} = 1\,\mathrm{eV}$ can be obtained. This situation corresponds to an axial frequency of $w_{\mathrm{z}} = 2\pi \times 0.88\,\mathrm{MHz}$ and radial frequencies of $w_{\mathrm{x}} = 2\pi \times 3.80\,\mathrm{MHz}$ and $w_{\mathrm{y}} = 2\pi \times 3.76\,\mathrm{MHz}$. However, this voltage set only creates a tilt of the radial modes of $3.6°$, reducing the effect of laser cooling parallel to the surface. Therefore, the voltage set applied to the DC electrodes during operation was adapted for better laser cooling conditions during trap operation, resulting in a lower trap depth [141].

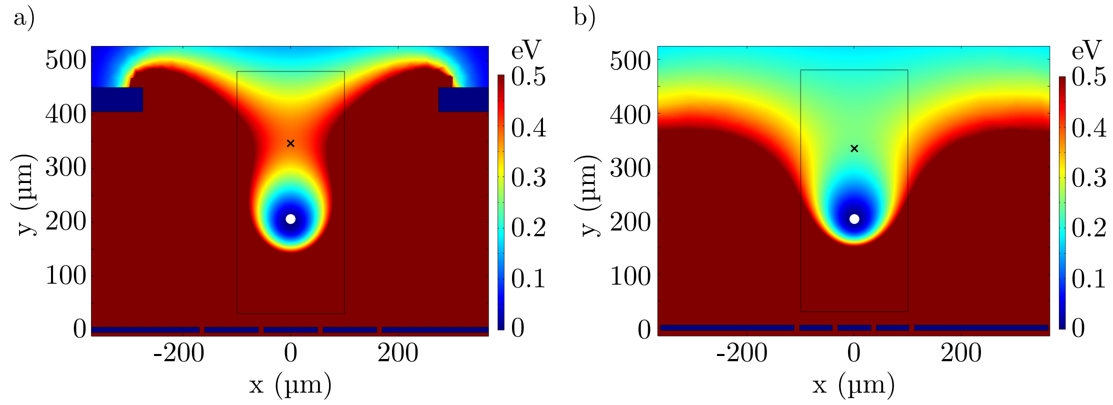

Figure 5.5: Pseudopotential generated in the a) hybrid trap or b) in a surface trap with the same ion-surface distance of 200 µm and an RF voltage of $V_{\text{RF}} = 200\,\text{V}$. To achieve the same ion-surface distance in the surface trap, the size of the electrodes was reduced while keeping the same ratio. The ion position is marked with a white dot, the saddle point with a black cross.

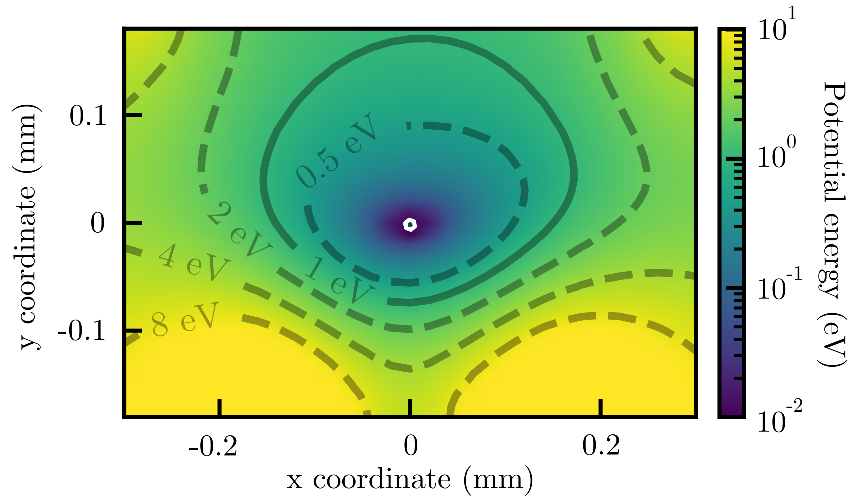

Figure 5.6: Potential energy of the hybrid trap for an RF voltage of $V_{\text{RF}} = 200\,\text{V}$ and the DC voltage set shown in table 5.2. The confinement potential exceeds 1 eV (solid line) as visible via the contour levels. Figure adapted from [141].

5.1.3 Routing and layer stack

The hybrid trap contains in total eleven layers on three wafers. The bottom layer of the hybrid trap has the same layer stack as the 2D trap presented in section 4.1.2. Three

Table 5.2: DC voltages used to operate the hybrid trap with shorted top electrodes for an RF voltage of $V_{\mathrm{RF}} = 183\,\mathrm{V}$ at a trap frequency of 20.6 MHz.

electrode	DC voltage (V)
A	7.66
B1 / B2	8.95
C1 / C2	17.18
1 (left side)	11.32
1 (right side)	12.77
2 (left side)	0.04
2 (right side)	-24.03
Top	10.46

metal layers separated by inter-metal oxide are deposited on a silicon substrate. The uppermost metal layer (metal 3) forms the DC and RF electrodes. The intermediate metal layer (metal 2) is used for routing the DC island electrodes to the bond pads. The lowest metal layer (metal 1) serves as a continuous ground plane for shielding of the substrate. The glass wafer separating bottom and top electrodes has a thickness of 400 µm. The top wafer is based on silicon on insulator (SOI) material, thus the top electrodes are made of conducting silicon. This 45 µm thick silicon layer is highly doped with phosphorus to provide a low resistivity of $1 - 2\,\mathrm{m}\Omega\,\mathrm{cm}$. The conductive silicon is separated from the 400 µm thick substrate silicon by 500 nm oxide, also referred to as buried oxide. A summary of the layer stack is given in table 5.3.

The electrical connectivity of the top electrodes to the carrier printed circuit board (PCB) is realized by etching the substrate silicon of the top wafer down to the conducting layer. The resulting $0.7 \times 1\,\mathrm{mm}$ large bond pads are coated with a stack of titanium (50 nm), platinum (100 nm) and gold (200 nm) to allow for wirebonding to this area. Wirebonds are either connected to additional bond pads on the bottom wafer or directly to the carrier PCB. For mechanical stability, the bond pads of the top wafer are residing on top of the glass spacer to avoid mechanical stress on the 45 µm thick conducting silicon layer during wirebonding. Scanning electron microscopy (SEM) images of the hybrid ion trap showing bond pads on top and bottom wafer as well as bottom island electrodes are depicted in figure 5.7.

To determine the compatibility of the highly-doped silicon forming the top electrodes with a cryogenic environment the conductivity was measured dependent on the temperature. The conductive behavior of silicon with respect to temperature depends

mainly on the degree of doping. With a lower dose of doping the ionization energy of the dopants cannot be reached at low temperatures, resulting in a "freeze-out" of the charge carriers. On the contrary, if silicon is doped in a high concentration, degeneracy is attained, leading to a good conductivity even at cryogenic temperatures [148]. Samples from a different technology sharing the same wafer material of 45 µm thick phosphorus-doped silicon were investigated. In the cryostat located at KAI (Kompetenzzentrum für Automobil- und Industrieelektronik) the resistance of the test sample was measured from room-temperature down to 16 K. The resistance dropped to around 70 % at cryogenic temperatures compared to the room-temperature value. This decrease demonstrates that the doping concentration is high enough to employ the hybrid trap's top layer as electrodes in a cryogenic environment.

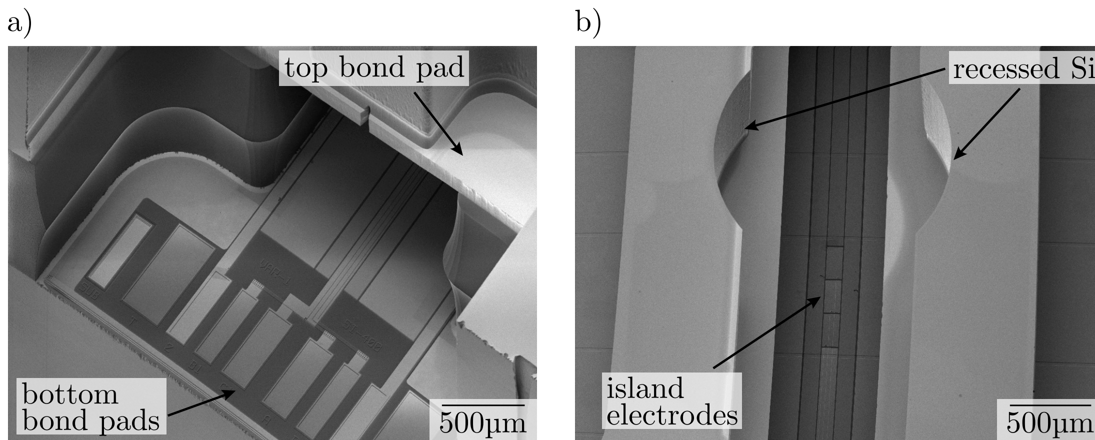

Figure 5.7: SEM images of the hybrid trap. a) The two top electrodes are contacted by using gold coated bond pads on the back side of the conducting silicon, where the substrate is etched. Electrical connectivity of the top electrodes is realized through wirebonding to the bond pads on the bottom layer. b) DC island electrodes in the bottom wafer, which are visible through the slit between the top electrodes, are routed in the underlying metal layer.

5.1.4 Design rules

For a successful fabrication of the hybrid trap, several design rules regarding structure dimensions have to be established and adhered to. These have to be considered already in the concept phase, to create a design compatible with the available fabrication methods. The following design rules are defined for the three wafers and the anodic wafer bond:

- **bottom wafer:** Because the bottom wafer of the hybrid trap shares the same layer

Table 5.3: Layer stack of the ion traps for the three wafers with material and thickness.

wafer	layer	material	thickness (µm)
top wafer	substrate	Si	400
	buried oxide	SiO_2	0.5
	top silicon	Si (highly doped)	45
spacer wafer	spacer	SiO_2	400
bottom wafer	metal 3	AlSiCu	2
	imox 2	SiO_x (deposited)	2.2
	metal 2	AlSiCu + TiN	1 + 0.025
	imox 1	SiO_x (deposited)	2.2
	metal 1	AlSiCu + TiN	0.75 + 0.025
	bottom oxide	SiO_2 (thermal)	1.3
	substrate	Si	725

stack and process flow as the 2D ion trap, the existing design rules as described in section 4.1.3 are adopted.

- **spacer wafer:** Structuring of the glass spacer is performed with an isotropic wet etch, thereby causing an under etch of the mask used for patterning. For the 400 µm thick glass wafer, the under etch is given by the etch depth of 280 µm. The optimum etch depth of 280 µm is given by the maximum etch time for smooth and accurate edges of the etched structures. At the same time sidewalls as vertical as possible can be achieved when etching the wafer from both sides to create holes. The uniformity of the wet etch is limited by the diffusion rate and thus reduced if the openings in the mask are too small. To avoid a drop in the etch rate for narrow structures, mask openings larger than 180 µm are recommended. This design rule combined with the expected under etch results in a minimum achievable hole diameter of 740 µm. A maximum deviation of ±30 µm from the target value for the etched structures is expected. Moreover, the total area of the wafer that is completely etched through should not exceed 30 % to maintain stability on wafer level, as experienced in a similar technology at Infineon.

- **top wafer:** The holes and cavities in the SOI top wafer are created by long deep reactive ion etching (DRIE) processes of the conducting silicon layer and the substrate silicon. In general, a DRIE process is able to achieve aspect ratios

of around 1 : 50 of etching depth to structure width. However, as soon as the aspect ratio is much larger than 1 : 1, the etch rate decreases strongly. Moreover, the minimum structure width to be resolved by optical lithography has to be taken into account as well: Because the trenches to be etched in the DRIE process are very deep, a thick resist that survives the long etching is needed. In this case, a 6 µm and 6.8 µm thick negative resist for the conductive silicon and the substrate silicon, respectively, are used as an etch mask. An experiment to test the resolution of structures of different widths in the 6.8 µm thick resist was performed to define design rules for the top wafer. Trenches can only be resolved from a structure width of 12 µm for the substrate silicon and 10 µm for the conducting silicon. Spacings between trenches, also called islands, can be resolved down to a minimal structure size of 5 µm. Moreover, if the wafer is etched in a large area, attention to the wafer-level stability needs to be taken, especially when the wafer is subjected to stress during processing. After fabricating the first top wafer of the ion trap, the openings of the wafer were reduced from 27 % to 14 % to gain mechanical stability, defining an additional design rule.

- **anodic wafer bond:** In the interface area, where the anodic bond is formed between two wafers, no residual oxide or metal structures are allowed, because the glass wafer can only bond to the silicon surface. This is especially important for the area in between the trap chips, where the alignment structures are placed which are used for the alignment process, overlay and control measurements during fabrication. At the position of these marks, cavities are needed in the glass wafer to bypass a disruptive topology in the interface that prevents bonding in this area. Air gaps in the bond interface are visible as Newton interference rings and reduce the bond quality. In figure 5.8 a picture of a void with interference rings is shown. This void is caused by a missing cavity in the glass spacer at the position of an alignment mark in the bottom wafer. Such air gaps typically have a thickness of a few micrometer and can also be caused by particles in the interface [149]. Residual air gaps in the bond interface of the ion trap could result in outgassing during trap operation in the cryostat. Therefore, the bond interface of the ion traps implemented in the experiment was characterized and no air gaps were detected on the devices. Furthermore, the interface area should have a minimum width of 120 µm to guarantee hermetic sealing.

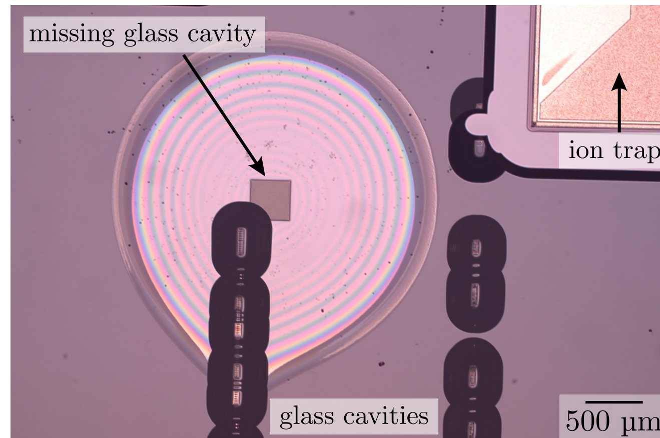

Figure 5.8: Glass wafer bonded to the bottom wafer, showing Newton interference rings indicating an air gap in the bond interface. This gap is caused by a lack of etching in the glass spacer at the position of an oxide structure in the bottom wafer. For other alignment structures, the glass is etched, visible as dark round areas.

5.2 Trap fabrication

In this section, the fabrication of the hybrid trap is described, which requires five wafers. The bottom, spacer and top wafer create the triple stack of the actual ion trap and are connected by wafer bonding. For the gold coating of the silicon top wafer two additional glass wafers are used as masks for shadow mask evaporation. The wafers are structured individually, followed by the anodic wafer bond. The single chips are separated by mechanical dicing.

5.2.1 Bottom wafer

The bottom wafer of the hybrid trap forms a surface trap, thus the layer stack and process flow of the 2D twin trap is used with an adapted layout. A detailed description of the structuring is provided in section 4.2.

As an additional process step of the bottom wafer fabrication the oxide in the bond interface is removed. For a reliable anodic bond between bottom and spacer wafer, a clean and oxide-free silicon surface is needed. Therefore, the oxide is etched in the interface area, which is located in the four corners of each trap chip (see figure 5.2) and the space between the individual trap chips. There are two possibilities to remove the oxide: by an anisotropic plasma etch, or by an isotropic wet etch.

For plasma etching, a resist mask is necessary, which covers all surfaces except the

intended bond interface during etching. The thermal oxide layer and the two layers of deposited tetraethyl orthosilicate (TEOS) add up to a thickness of 5.7 µm, resulting in a very long etching time of 700 s, compared to common processes on the used etch tool. Because of the high thermal stress of the etching equipment, the wafer needs to be processed in two runs of 350 s each. The plasma etch shows a homogeneous oxide etch over the whole wafer surface without any residual oxide.

When using a wet etch to remove the oxide in the interface area, the AlSiCu of the metal 3 layer can be used as a hard mask for structuring due to the high selectivity of the etching solution of 1 : 40 for aluminum and oxide. Therefore, no additional lithography step is needed. Moreover, this etching technique allows for etching the oxide in the gaps between the electrodes, reducing the amount of exposed oxide in the trap. Due to the long etch time of 90 min, the under etch of the electrodes reaches ∼7 µm (see also figure 4.11), reducing mechanical stability. Therefore, bending of the free-standing electrodes during dicing cannot be prevented, leading to shorts between electrodes in the worst case.

In order to achieve both a wafer surface etched down to the substrate and under-etched electrodes without exposed oxide, we combine the two methods of plasma and wet etching in a two-step process. First, half of the interface oxide is removed by plasma etching. Second, a wet etch is performed to remove the residual interface oxide, that simultaneously etches the oxide in the gaps down to the metal 1 shielding layer. Still, this procedure is limited by the inhomogeneous etch rate over the wafer surface of the wet etch, showing a faster etch rate at the wafer center. As a result, a residual thin oxide layer is observed as a ∼5 cm wide ring along the wafer edge, preventing an anodic waferbond in this area. Figure 5.9 depicts the bottom wafer with and without a residual oxide ring at the wafer edge. Out of the different methods of oxide etching presented here, pure plasma etching shows the best results in terms of oxide-free interface for a successful wafer bond. For this reason, the plasma etch process was chosen for the hybrid trap, although under etched electrodes are dispensed in this case.

5.2.2 Spacer wafer

The spacer wafer is made of borosilicate glass (MEMpax®) and defines the distance between bottom and top electrodes. To achieve a suitable coefficient of thermal expansion (CTE) matched with the silicon wafers, the glass is modified with sodium. These sodium contents lead to a different contamination classification compared to the standard silicon, limiting the toolpark of available fabrication processes in the Infineon production line. Wafers with different contamination classifications are not allowed to use the same tools and equipment to prevent defects and yield loss.

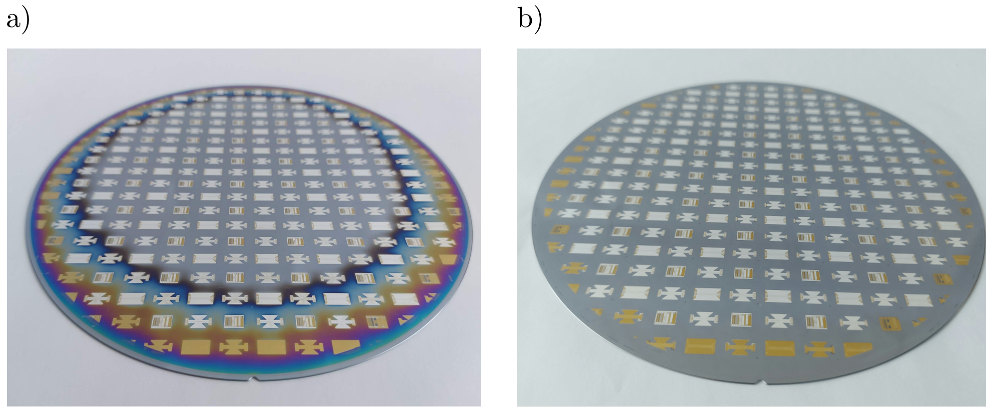

Figure 5.9: Bottom wafer of the hybrid trap. a) The interface oxide is etched by a two-step process starting with a plasma etch followed by a wet etch. Residual oxide is visible through a rainbow colored ring on the wafer edge. Only the wafer center is oxide-free (gray). b) The interface oxide is removed by plasma etching, resulting in a homogeneously etched silicon surface in the interface area.

The first fabrication step of the glass spacer is a coating with 80 nm amorphous silicon through low-pressure chemical vapour deposition (LPCVD). This layer forms a hard mask for the isotropic wet etch. To create holes through the wafer for optical access in the ion trap, we need to structure the wafer from both sides. We perform optical lithography first on the top side and subsequently on the bottom side with a positive resist mask of 1.9 µm thickness. After curing the resist by baking, the amorphous silicon is structured by plasma etching. The remaining silicon pattern forms the hard mask for the following isotropic wet etch of the glass. After removal of the hard mask and several cleaning steps, an automated optical control with SEM measures the width of the etched structures in multiple areas on the wafer to provide feedback and hence process control for the wet etch process.

Because the ion trap requires the glass to be removed at the trapping site and all lateral sides for laser access, the wafer is etched to a depth of 280 µm from both the top and the bottom side to create holes in the 400 µm thick glass wafer. Thus, a large amount of glass is etched during structuring, resulting in an open area of around 30 %. Despite this value reaching the limit defined from internal experience for the maximum etched area, reliable wafer stability is still observed. The isotropic etch leads to a 85 µm wide spike in the center of the sidewall, as depicted in figure 5.10. The structured glass spacer and an SEM image of its cross section are also shown in figure 5.11.

Figure 5.10: Isotropic etch of the 400 µm thick glass wafer (blue). The wafer is either etched from both sides, to create the opening for the ion trap (left), or only from one side, to create a 280 µm deep spherical opening above alignment structures in the bottom wafer (right). Etching from both sides results in a 85 µm spike.

5.2.3 Top wafer

To form the necessary holes for optical access in the SOI top wafer, it needs to be etched through completely. To achieve the desired trenches in the 45 µm thick conductive and 400 µm thick substrate silicon layer, a DRIE is used. After structuring, a coating with titanium platinum gold (TiPtAu) is done on both sides of the wafer by shadow mask evaporation to reduce the amount of silicon in direct line-of-sight to the ion and create a metallic surface to allow for wire bonding to the electrodes. The fabrication of the top

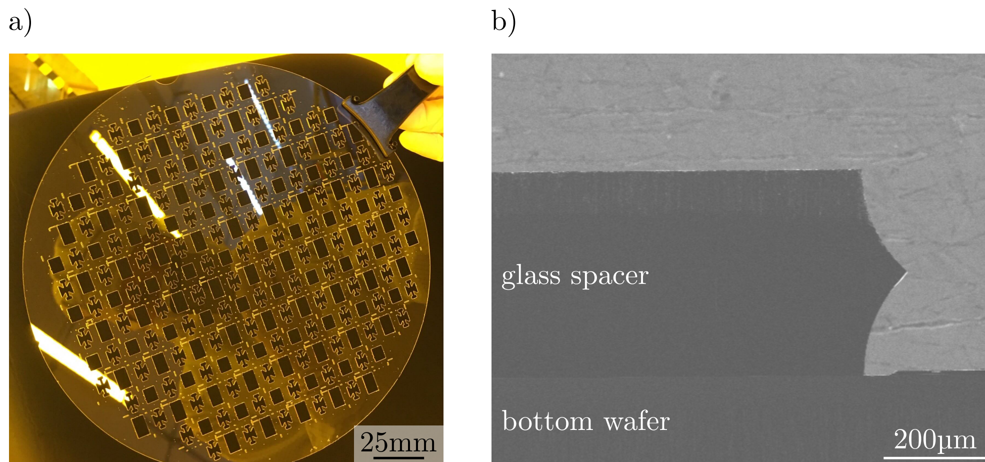

Figure 5.11: a) Glass spacer wafer of the hybrid ion trap. Holes are structured by isotropic wet etching, resulting in an etched area of around 30 % of the full wafer. Despite the large etched area, the wafer shows a high stability on wafer-level. b) SEM image of the glass wafer (dark gray) bonded to the bottom wafer.

wafer is challenging because the area that needs to be etched through is very large to allow for optical access for camera and lasers, and create openings above the wirebond pads. For this reason, the mechanical stability of the wafer is reduced. If mechanical stress becomes too high during processing, wafer breakage may occur.

Deep reactive ion etching

The basic fabrication flow of the top wafer is illustrated in figure 5.12. First, a protective oxide (TEOS) layer is deposited on the front side of the wafer to avoid scratches and etching during the back side processing. With optical lithography, a negative resist is applied as a mask for the DRIE. Then, the protective oxide is removed in the patterned areas, followed by the DRIE. The DRIE process consists of three alternating steps: passivation of all surfaces, removing the passivation layer with ion sputtering on all horizontal surfaces, and an isotropic etch of the silicon. The C_6F_8 polymer passivation coats the sidewalls to avoid etching during the isotropic silicon etch. This passivation layer needs to be removed by reactive argon ion sputtering, before the silicon is isotropically etched with SF_6 for a short time period. This procedure is repeated until reaching the oxide separating the conductive and substrate silicon. The wafer is flipped and the same process steps with optical lithography and DRIE etch are performed on the back side of the wafer. Afterwards, the protective oxide layer as well as the residual buried oxide in holes and the bond pad area is removed by a wet etch to reduce the amount of exposed oxide to the trapped ion during operation.

The first batch of samples had an open area of 27 % etched through completely, causing insufficient mechanical stability and consequent wafer breakage during the back side DRIE. The first attempt to add mechanical stability was to temporarily bond a silicon handling wafer to the top wafer. With this double wafer stack, the DRIE could be performed without causing wafer breakage. However, this method was not suitable, since the wafer could not be detached after etching without damaging the top wafer. The solution was found in reducing the total number of structures. A reduced open area of around 14 % turned out to be sufficient to provide enough mechanical stability. In figure 5.13 a top wafer broken during DRIE as well as a successfully fabricated wafer with structures only in the wafer center are depicted.

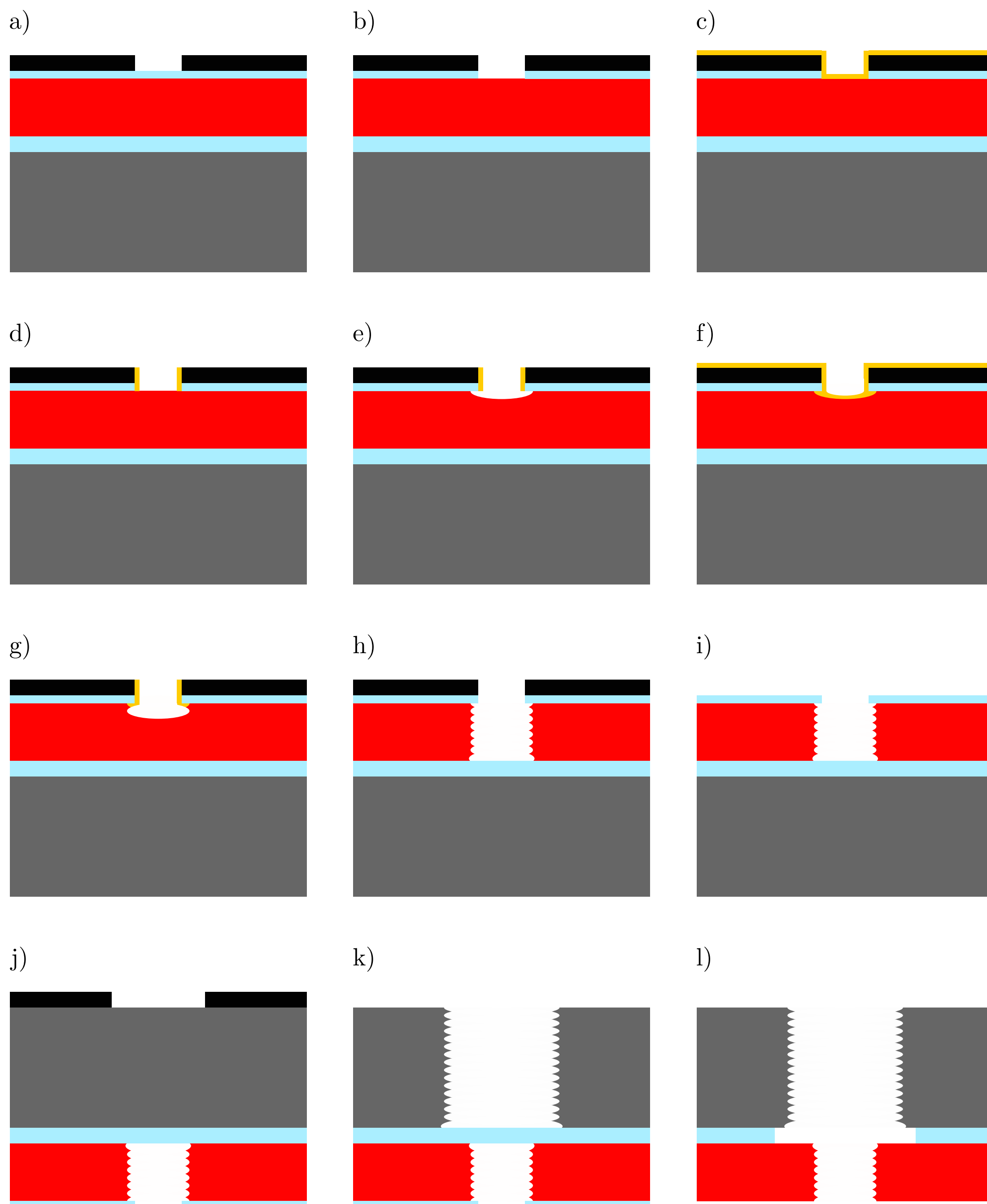

Figure 5.12: Fabrication steps of the top wafer. a) Resist mask (black) applied with optical lithography, b) oxide (blue) etch, c) DRIE of the highly doped silicon (red), starting with a polymer passivation with C_6F_8 (yellow), d) ion sputtering with reactive argon ions, e) isotropic etching with SF_6, f) passivation, g) isotropic etching, h) resulting trench with scallops, i) resist strip, j) backside structuring of the substrate silicon (gray) starting with a resist mask (black), k) backside trench down to the buried oxide, l) isotropic oxide etch.

a) b)

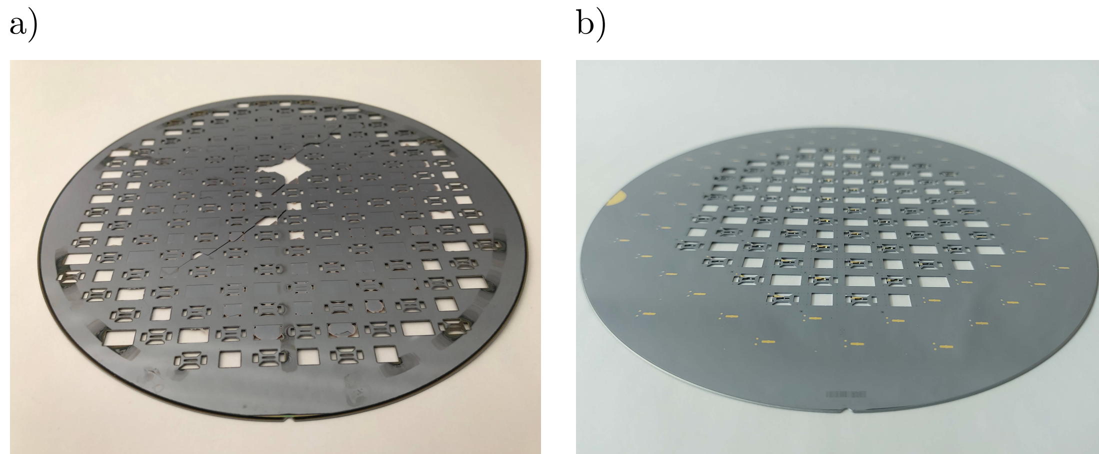

Figure 5.13: Structured top wafer. a) Wafer breakage during the backside DRIE. The wafer breaks along the diagonal, along the crystallographic 100 axis. b) Keeping the outermost devices solid in the area along the wafer edge increases stability and prevents the wafer from breaking. The etched area is reduced from 27 % to 14 %.

Shadow mask evaporation

To avoid micromotion induced by stray charges in the silicon surface, the areas closest to the ion are coated with a stack of titanium, platinum and gold. The gold coating needs to be done as the last process step because gold is classified as critical material and therefore not permitted in the DRIE tools. Hence, the gold coating is performed after the second DRIE etch that creates holes through the whole wafer. These holes prevent from using optical lithography. Therefore, neither a lift-off process nor electroplating is available for the gold coating.

For this reason, a shadow mask evaporation is used for coating the desired areas. This process is realized by using one glass wafer each as shadow mask for the front and for the back side of the top wafer. These are fabricated similar to the glass spacer wafer described in section 5.2.2. The evaporation is performed in two steps, starting with the front side of the top wafer. The shadow mask is semi-automatically aligned and temporarily bonded to the top wafer with multiple revalpha sticks[1] distributed over the interface. Then, the wafer is evaporated with successive layers of 50 nm titanium, 100 nm platinum, and 200 nm gold. Titanium serves as an adhesion layer and platinum as a diffusion barrier for the gold layer. After evaporation, the shadow mask is removed by heating up the wafer to above 150 °C until the thermally-releasable revalpha sticks

[1] thermal release tape

detach. These process steps are repeated for the back side of the wafer. The resulting gold structures on the top wafer are shown in figure 5.14.

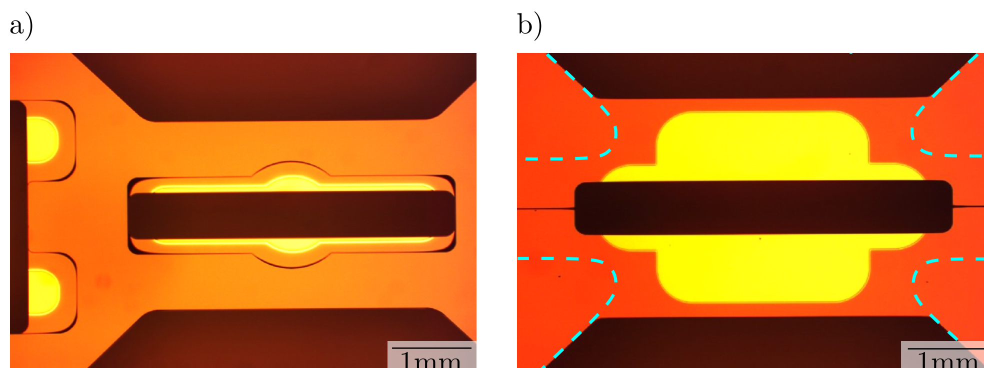

Figure 5.14: Microscope image of the top wafer with gold coating through shadow mask evaporation. a) Top side with gold coating (yellow) of the bond pads (on the left) and the inner area of the electrodes, where the substrate silicon is recessed. b) Back side with gold coating in the area closest to the ion in the trap. The position of the glass pillars connecting the top and bottom wafer is indicated with a blue dashed line.

5.2.4 Wafer bonding

After structuring the individual wafers, a wafer bond process connects the three wafers. In general, a variety of different wafer bonding techniques, which are available at the Infineon production site in Villach, could be applied to the ion trap wafers, such as fusion bond [150], anodic bond [34], eutectic bond [151], thermo-compression bond [152], glass-frit bond [153], and adhesive bond [154]. Considering the design rules of the hybrid trap and potential benefit from experience gained in other productive technologies with a similar wafer stack at Infineon, we decided to use an anodic bond for the ion trap triple stack. As an alternative, a eutectic bond was investigated as a back-up plan.

Anodic wafer bonding

Anodic bonding was first introduced by Wallis and Pomerantz in 1969 [34] and is now widely used in industry, especially in packaging and manufacturing of sensor systems [155, 156]. The most commonly used material combination is borosilicate glass and silicon. It is suitable for various applications due to high bonding strength and because there are no high demands on the bond interface in terms of flatness and cleanliness of the environment for successful bonding [157].

For the anodic bond process, the glass wafer and silicon wafer are put into close contact between two graphite electrodes. Then, a positive voltage is applied to the anode that is connected to the silicon wafer. Due to the voltage, alkali ions (mostly sodium) in the glass wafer start to migrate towards the cathode. This ion migration forms a depletion zone in the glass wafer at the interface to the silicon, around $100 - 1000\,\mathrm{nm}$ wide. With an increasing width of the depletion zone, the electric field in this layer increases until the activation energy for oxigen anions in the glass wafer is reached. The anions start migrating towards the anode. When arriving at the silicon interface, they form covalent bonds with the silicon atoms, creating the bond between the glass and silicon wafer. In figure 5.15, the anodic bond process is shown.

In the glass wafer, three regions are formed during the anodic bond process: the depletion layer at the silicon interface, followed by bulk glass, and the region close to the cathode (pile-up layer), where the migrated alkali ions accumulate.

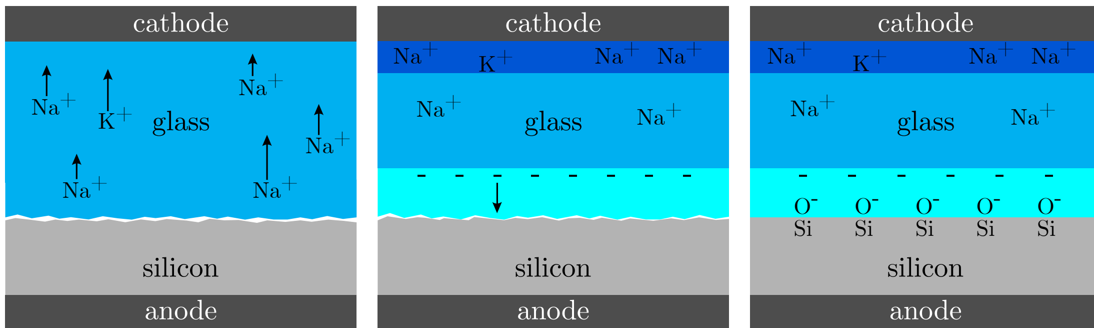

Figure 5.15: Anodic bond process for a silicon-glass interface. When applying a positive voltage to the anode, ion migration of alkali ions in the glass (blue) towards the cathode is triggered, forming the pile-up layer (dark blue). This migration generates a depletion zone with anions at the wafer interface (light blue). As soon as the activation energy of the anions is reached by the electric field in the depletion zone, the anions start moving towards the anode until they arrive at the interface. Here, covalent bonds of the oxygen anions with silicon are formed, creating the bond between the two wafers.

Triple-stack anodic waferbond

For the hybrid trap, two glass-silicon interfaces need to be wafer-bonded. In principle, this bond can be done in one step by switching the role of the two graphite electrodes or contacting the inner glass wafer laterally on the wafer edge to connect it to the cathode, which is already used in MEMS applications [158]. However, a simultaneous alignment of both interfaces is difficult because the silicon wafers on the outer sides of the triple

stack are not transparent. Thus, a pre-bond to fixate two wafers is necessary. This pre-bond is performed by laser irradiation of a small area in the wafer center to create a spot welding of the melting glass to the silicon and allows for aligning the third wafer to the fixed double stack. Unfortunately, attempts to conduct a pre-bond on the hybrid trap wafers were not successful, because the interface area used for the pre-bond is too small for a sufficient adhesion of the two wafers. Since the necessary layout modification would have taken too much time, we decided to split the wafer bond process into two steps. First, the bottom wafer is anodically bonded to the glass spacer, followed by the bond of the top wafer to the double stack.

One challenge in bonding the glass wafer from both sides is the pile-up zone formed during the first bond. The ion migration of alkali ions in the glass spacer towards the cathode leads to a sodium contamination on the glass wafer surface. This can result in a weaker second bond or, in the worst case, prevent successful bonding of the second interface. Test bonds with a cleaning step for the spacer wafer between the first and second anodic wafer bond were conducted and analyzed, but no further improvement of the bond quality was observed (details on bond quality are given in section 5.3.3). Thus, no additional cleaning step for alkali removal was integrated in the wafer bond routine.

A precise alignment of the top electrodes to the bottom electrodes in the hybrid trap is crucial to avoid micromotion that cannot be compensated. The alignment accuracy of around $3 - 4\,\mu\text{m}$ for each interface results in a maximum displacement of $8\,\mu\text{m}$ of top and bottom electrodes. This leads to a shift of the RF null $\leq 1\,\mu\text{m}$ and a negligible change in motional frequencies, as discussed in detail in [111]. The spacer wafer is aligned to the bottom wafer in the first bond, followed by an alignment of the top wafer to the spacer wafer in the second bond. To guarantee a minimal displacement in the x/y direction and a minimal tilt of the two wafers, they are aligned in a semi-automatic alignment process. Alignment marks at two opposed locations on the wafer surface close to the wafer edge are used for this process. In the bonding tool, the two wafers are aligned semi-automatically with help of a microscope. Then, the wafers are handled automatically by the bonding tool to bring them in contact while keeping in the aligned position. The wafer stack is then temporarily fixed with clamps at the wafer edge before entering the bond chamber.

Because the exact bond process needs to be adapted for every application, first a series of bond tests with 10 waferstacks was performed to find the optimal bond parameters for the triple stack creating the hybrid trap. For these tests, the voltage amplitude, ramp-up time, cleaning steps, and chamber environment were modified in a process matrix to evaluate a stable parameter set. Out of this pre-runner experiment, a suitable anodic bond process for the hybrid trap was developed. Crucial bond parameters

cannot be provided to protect proprietary IP. The procedure includes five steps:

I) **Heating**: The first process step after loading the two wafers into the bond chamber is heating. The temperature of the top and bottom wafer are rising.

II) **Bond preset**: Since the bond is done in high vacuum (HV), the chamber needs to be pumped until the chamber pressure reaches the target pressure. Moreover, the top electrode is lowered until it is in contact with the upper wafer in the chamber without active pressure. This allows removing the clamps.

III) **Pressure build-up**: Next, the pressure of the top electrode to the wafer stack is increased, to facilitate a low electric resistance contact [155]. The final bond temperature is now reached and the top electrode is switched on.

IV) **Voltage influence**: The voltage of the top electrode is ramped-up to the final bonding voltage. In this step, the bond in between the two wafers is formed. When ramping-up the voltage too fast, plasma discharging and voltage drops were observed during the pre-runner bond tests. Therefore, the ramp-up is kept slow and the maximum voltage is set to a relatively small value compared to other technologies.

V) **Cool-down**: After the bond is performed, the chamber is flooded with nitrogen to increase the chamber pressure. The top electrode is lifted from the wafer stack. After a waiting time for cool-down the wafer stack is unloaded.

This procedure is used for both bonds, first forming a double-wafer stack and finally a triple-wafer stack. The bond quality is investigated using different approaches, as described in section 5.3.3.

Alternative: eutectic bonding

Although several tests were performed to examine the applicability of the anodic bond to the hybrid trap wafers, a eutectic bond was developed as a back-up plan. Eutectic bonding takes advantage of the low melting point of certain metallic alloys. When reaching this temperature, where both metals melt on the interface, a permanent bond is formed. When using a gold-silicon interface, the melting point reduces from 1063 °C (Au) and 1412 °C (Si) to 363 °C [151], which is compatible with the allowed thermal budget of the ion trap wafers.

This method requires an additional gold coating of the glass spacer wafer instead of the bare glass surface. Therefore, the structured spacer was evaporated with a thin layer of 50 nm titanium and 100 nm platinum below a 1000 nm thick gold layer.

Titanium serves as adhesive and platinum as a diffusion barrier for the highly mobile gold atoms. In figure 5.16, the gold-coated spacer wafer as well as a cross section of the bond interface is shown. Research on this technique has been performed by Lina Purwin and is available in her master thesis [159].

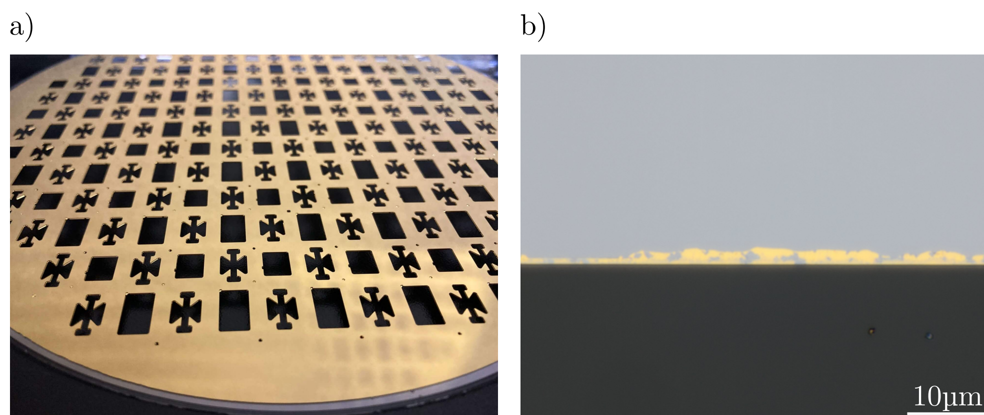

Figure 5.16: a) Gold coated spacer wafer used to form a eutectic bond to the silicon bottom and top wafer. b) Microscopic image of the interface after eutectic bonding of the ion trap wafers. The gold (yellow) on the glass wafer (dark gray) diffused into the silicon wafer (bright gray), forming a permanent bond.

Eutectic bonding might be relevant for future large-scale 3D ion traps, because it enables electrical connections between top and bottom wafer through the glass spacer. Such a connection could be realized either by a simple sidewall metallization, or by through-glass vias (TGVs). An integration of through-glass via also helps with scaling up the number of electrodes on the top wafer, as described in chapter 6.

5.2.5 Dicing and Packaging

The separation of the individual chips for the hybrid trap is challenging, since the wafer stack is exceptionally thick with around 1.5 mm compared to a standard wafer thickness of 725 µm. After careful consideration and discussions with experts, mechanical dicing was decided to be the most suitable method to neither damage the ion trap chips nor the dicing tool.

The wafer stack is laminated on a UV-releasable foil fixed in a dicing frame to ensure that the single chips stay in position after separation. Because the wafer stack is rather heavy, the lamination needs to be done manually. No issues such as tape sagging over time occurred. Due to the large thickness of the wafer stack, non-standard sawing blades with 120 µm width are necessary to dice through the whole wafer, while the width of

the sawing line is restricted to 200 µm. To guarantee a full separation of the ion traps, the stack is diced up to $20 - 30$ µm into the underlying foil. After dicing, the wafer is illuminated with UV light to weaken the adhesion of the single chips to the foil to simplify detachment.

For the dicing process, the following challenges and risks have been identified during the concept phase:

- challenge to create an automated dicing setup with alternating distances between dicing lines due to the different chip sizes of the productive structures and filling area for mechanical stability of the wafers
- risk of breakage of the sawing blade due to the large thickness of the wafer stack
- risk of flying dies (detached structures or chips mainly at the wafer edge) due to a bad wafer bond and/or dicing through cavities in the glass spacer and top wafer

Nevertheless, a semi-automatic dicing procedure was successfully developed for the hybrid traps. Similar to the 2D twin trap, a jet of water with a small addition of Stayclean-F cleaning agent was used to rinse off dicing debris immediately, as described in section 4.2.4. Although the sawing blade broke while dicing some wafers, no major consequences for the ion traps and the dicing tool were observed. Flying dies occurred mainly at the wafer edge, where they are less harmful compared to the wafer center, where they could scratch productive ion trap chips.

An industrial packaging for the hybrid trap was developed, including glueing to a PCB and wirebonding for electrical contact. Details on the automated assembly process and the Infineon carrier PCB are given in section 4.2.5. When the first ion traps were fabricated, the cryogenic setup at ETH Zurich used for the characterization was not fully compatible with the PCB developed at Infineon. Therefore, the hybrid traps were glued to PCBs designed by colleagues at ETH. Because there are leads located in the area below the trap chip on the ETH carrier PCB, a non-conducting glue (ABLEBOND® 2025M) was used to avoid electrical shorts in between trap electrodes. Each bond pad was wirebonded to the PCB with two 25 µm thick gold wires. The top electrodes were directly wirebonded to the PCB. Later on, an adaptation of the ETH setup enabled mounting ion traps assembled on the Infineon carrier PCB. These traps were glued with the same Infineon-proprietary conductive glue as used with the 2D twin trap. In figure 5.17, a diced triple stack wafer and a wirebonded ion trap on the Infineon carrier PCB is shown.

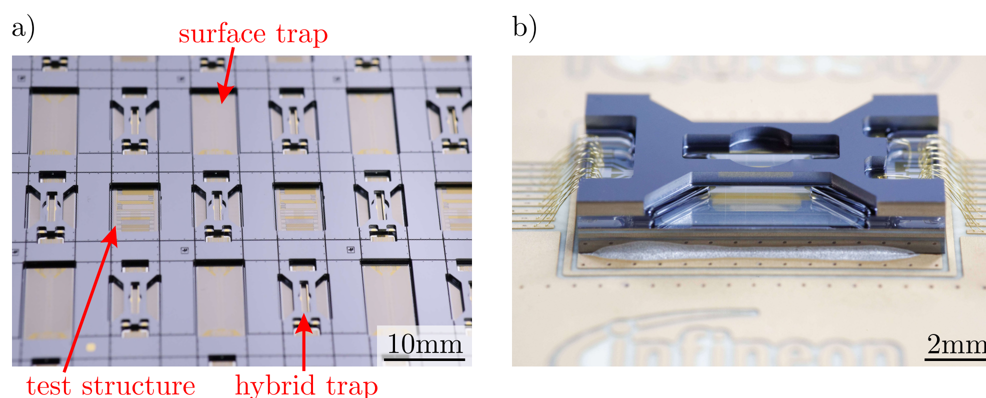

Figure 5.17: a) Mechanically diced ion traps, visible as a grid of thin, black lines. Beside the hybrid traps with top layer, a surface trap design as well as electrical test structures are fabricated on the same wafer. b) Hybrid trap glued and wirebonded to the Infineon carrier PCB.

5.3 Quality analysis

Before testing the performance of the hybrid trap in the experiment, numerous measurements and analyses were carried out for inline process control, electrical behavior and material properties of the ion trap. These tests include in-line measurements during fabrication, as well as electrical and optical analyses conducted in the failure analysis (FA) department of Infineon in Villach. Moreover, four different tests to determine the wafer bond quality were performed.

5.3.1 Inline measurements

During fabrication, in total 39 measurements are performed on the three ion trap wafers to guarantee reliable and reproducible devices. Measurements of the layer thickness, alignment measurements between subsequent layers, automatic SEM analysis of etched structures, wafer bow measurements as well as visual controls to immediately detect possible deviations are conducted at defined process steps in the fabrication routine. These control steps account for around 30 % of all processes performed on the wafers. The measured values are automatically stored and can be retrieved at any time for analysis and statistics.

Critical-dimension measurements

Automatic SEM measurements are performed to determine the width of the structured resist acting as an etching mask as well as width of the etched structures themselves.

Typically, five measurement points are taken for one wafer of each lot (one lot contains 1 - 24 wafers). If the measured value is out of the specification range, the processing of the wafer is immediately stopped to allow for a detailed analysis of the deviation. Such measurements are referred to as critical dimension measurements and are integrated for every layer of the ion trap. For instance, the target structure size of the resist mark for the plasma etch of the the metal 1 layer is 0.95 µm. Specification limits are ±0.15 µm for this mark. In figure 5.18, the corresponding values for this critical dimension measurement are presented in chronological order for every lot fabricated as an ion trap bottom wafer. All measured values are clearly within specification.

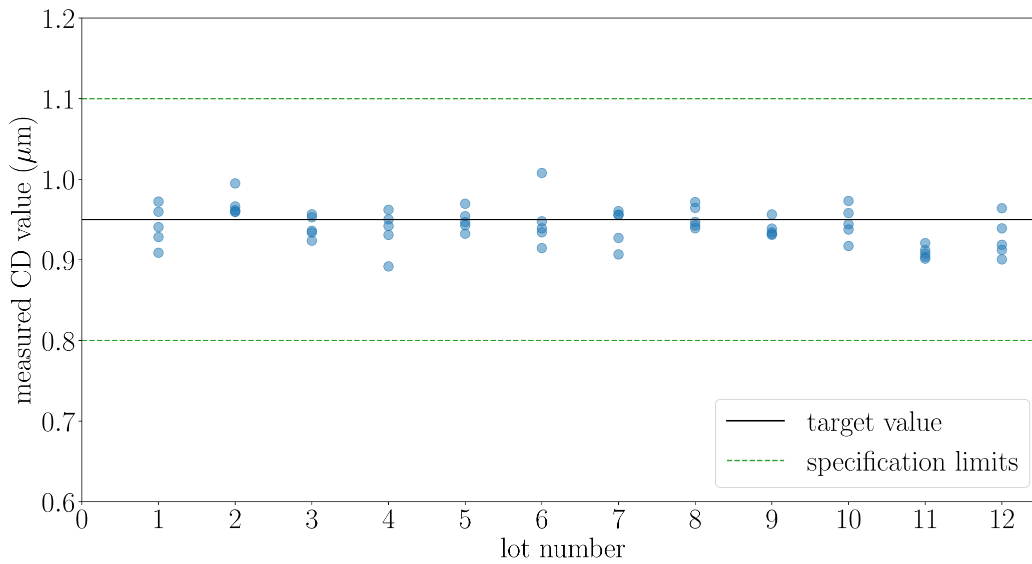

Figure 5.18: Data of the automated critical dimension measurement of the resist mask for the metal 1 layer of the bottom wafer. Each lot of up to 25 wafers is characterized by five fully-automated SEM measurements performed on one of the wafers. Measured lots are presented in chronological order. All measured points are well within the specification limits of 0.95 µm ± 0.15 µm (green dashed lines) of the target value (black line).

Automated electrical wafer test

Another very useful measurement tool integrated in the process flow of the hybrid ion trap is a fully-automated electrical wafer test. Here, the RF lines of every chip are tested for breakdown voltage and leaking currents. Every wafer with the same layout is measured by automatically stepping the probe needles aligned to the bond pads from

chip to chip. DC voltages up to 600 V are available for this test. The test also provides the failure description, as for example lack of contact, algorithm fail, arcing, high current or error during measurement.

The measurement is performed at atmospheric pressure, thus arcing between electrodes is expected from voltages $\approx$ 327 V for gaps with 7.5 µm width according to Paschen's law [160]. For both larger and smaller gap widths arcing should occur at higher voltages. For the hybrid trap, we integrated a simple wafer test for the bottom wafer, where the leakage current between RF and ground is measured up to 300 V in steps of 50 V. The distance between RF and ground electrodes is 4.4 µm. Therefore, the chips are not damaged and still available for ion trap experiments. The measurement sequence starts with a Kelvin test to check the initial contact of the probe needles to the bond pad. For instance, a lot with 10 wafers contains 1140 ion traps. Out of these traps, 1108 traps successfully passed the wafer test, corresponding to 97.2 % yield. The main reason for the failure was the absence of the metal 3 layer forming the electrodes on some chips at the wafer edge. Thus, the chips failed already in the Kelvin test at 50 V. The results of the wafer test are presented in figure 5.19. Only chips that passed the wafer test are provided to the ion trap experiment.

5.3.2 Surface characterization

Since the ion trap performance depends strongly on the surface conditions of the electrodes and surrounding surfaces, the surface roughness and cleanliness are characterized on the ion trap wafers. Rough surfaces can lead to scattered stray light from lasers reducing the detection reliability, whereas contaminations like adsorbents on the trap surface create stray electric fields.

Surface roughness analysis

A characterization of the surface roughness of the ion traps was performed in the FA of Infineon Villach using an atomic force microscopy (AFM) analysis. In surface ion traps, where the ion-surface distance is in the range of a few tens to a few hundreds of micrometers, a rough trap surface can lead to stray laser light causing detection errors. Therefore, a smooth trap surface is preferred.

First, the surface roughness of the AlSiCu metal layer providing the trap electrodes was measured. Structured chips from the bottom wafer with the full layer stack were used to get realistic values. An AFM analysis of the metal surface performed on a 60 µm $\times$ 60 µm square revealed a root-mean square roughness of $\sim$ 30 nm. The measured surface pattern is shown in figure 5.20.

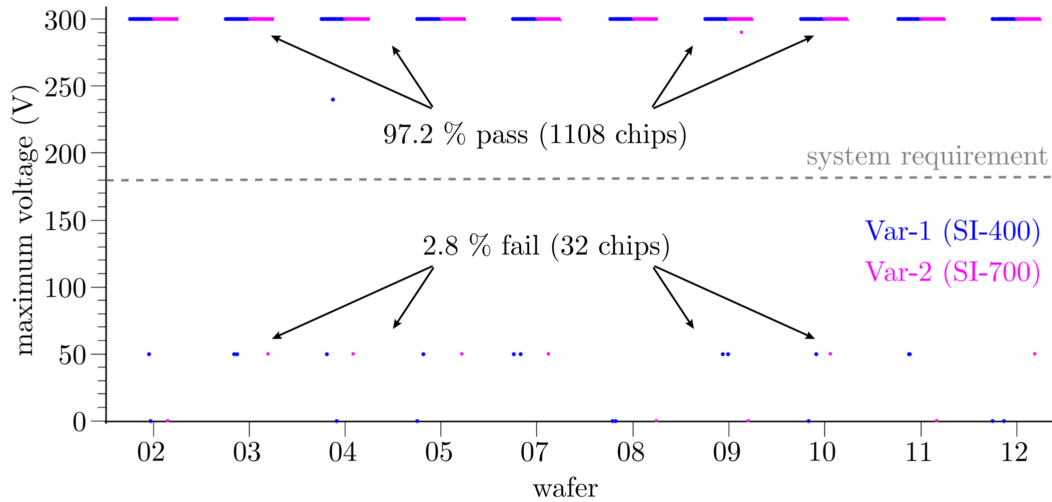

Figure 5.19: Data of the automated wafer test on the ion trap bottom wafers. Plotted is the voltage, at which a leakage current was detected. If no leakage current was observed, the data point was set to 300 V. The system requirement of 180 V is marked with a gray dashed line. Both versions of the hybrid trap were tested (SI-400 and SI-700). 97.2 % of all chips passed the test. Most fails occurred during the initial Kelvin test at 50 V, when the contact of the probe needles to the bond pads was tested. This lack of contact is caused by the absence of the metal 3 layer on some chips at the wafer edge.

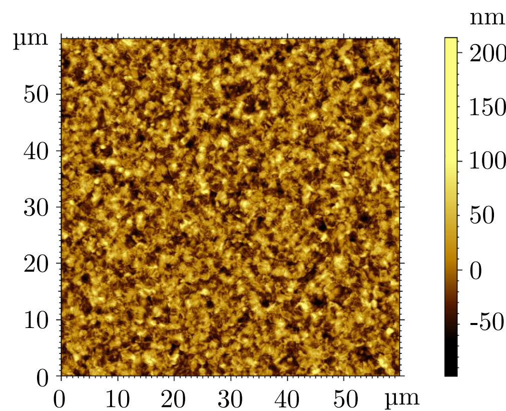

Figure 5.20: AFM of the AlSiCu surface of the ion trap. The full layer stack adds up to a root-mean square roughness of ~ 30 nm.

Moreover, the roughness of the silicon and glass surface forming the interface for the anodic waferbond was measured. For successful anodic wafer bonding, the substrate surfaces need to be flat, smooth and clean. The surface roughness of the bond interface should not exceed 50 nm to enable hermetic sealing of the two wafers [149]. The silicon

surface roughness was measured on 6 different positions on the bottom wafer interface. In this area, the thermal and deposited oxide was removed by plasma etching. A roughness of 3.7 nm was measured in the wafer center, increasing to 9.1 nm close to the wafer edge. The measured average roughness is around 6.4 nm. In a similar way, the roughness of the borosilicate glass wafer was determined on 3 points from the wafer center to the wafer edge, where the roughness increases from 13.5 nm to 16.6 nm. These values indicate a suitable basis for successful wafer bonding.

Surface cleanliness analysis

An attempt to remove the oxide in the gaps between electrodes with an isotropic etch was conducted. Removing exposed oxide could help minimizing micromotion of the trapped ion. To protect the electrodes from the powerful water rinse during dicing, the whole triple stack wafer was spin-coated with a protective resist. When removing the resist before wirebonding, spots on the metal electrodes were observed. These spots were only located in the area, where the metal was coated with resist.

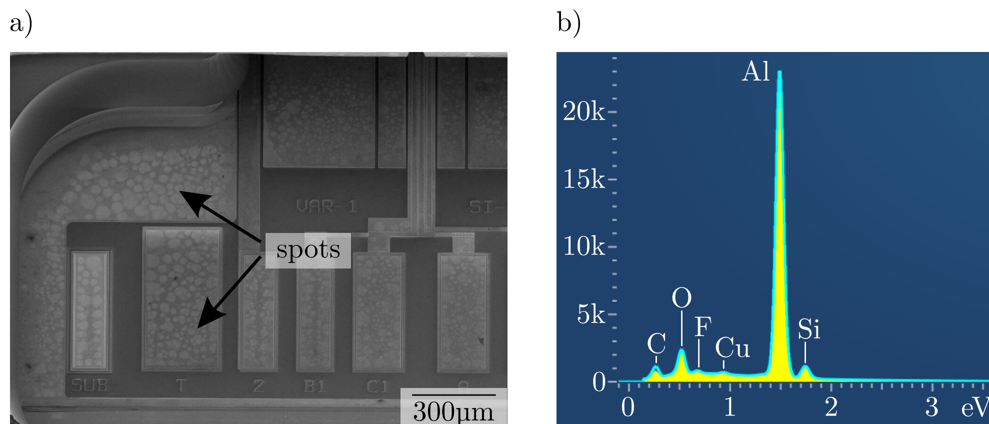

Figure 5.21: a) SEM image of the bonded ion trap, showing spots on the AlSiCu metal surfaces of the bottom wafer. b) EDX analysis of the spots, revealing contamination with fluorine. In combination with hydrogen, hydrofluoric acid is formed, etching the aluminum of the metal surface. This creates small holes on the metal surface, visible as spots in the SEM picture.

With an energy dispersive X-Ray analysis (EDX) contaminants on the trap surface were determined. In this analysis method an electron beam excites atoms that emit characteristic X-rays which are used to identify the composition of elements of the sample [161]. This analysis revealed residues of fluorine. The suggested hypothesis for this appearance is that after the long oxide etch some flourine residues from the etching

solution remained on the AlSiCu surface. When coating the wafer with protective resist, the fluorine residues form hydrofluoric acid (HF) with the organic resist. The hydrofluoric acid then etches some small amount of aluminum of the AlSiCu surface. This creates small holes on the metal surface, which are visible as on the electrodes and bond pads. In figure 5.21, the spots on the trap electrodes and the results of the EDX analysis are shown.

To circumvent this problem, various methods have been developed to, on the one hand, mechanically stabilize the electrodes, and, on the other hand, seal the surface with a protective metallic layer. Mechanical stabilization eliminates the need to apply a protective coating for the dicing process. The electrodes in metal 3 can be stabilized by additional (intermediate) layers of TiN or TiW. Such metal layers on top of the metal 3 surface also have the advantage of preventing the AlSiCu to react with HF, if the wafer is coated with protective resist. In figure 5.22 an ion trap with additional TiW coating and without visible spots is shown.

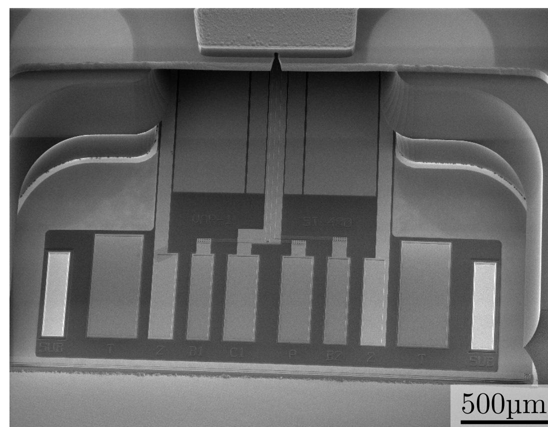

Figure 5.22: SEM image of the bonded ion trap without spots on the AlSiCu metal surface due to a protective TiW layer on the electrodes.

5.3.3 Waferbond characterization

The anodic wafer bond needs to withstand mechanical and thermal stress during mounting and operation of the ion trap. Therefore, several quality tests were performed to demonstrate suitability of the anodic wafer bond for the ion trap and experiment operation.

Confocal scanning acoustic microscopy analysis

One method to verify a bonded interface after wafer bonding is confocal scanning acoustic microscopy (CSAM) analysis. Acoustic waves are used to find defects like cracks or voids in the bond interface. The wafer is placed in a liquid medium (e.g. purified water to avoid deposition of residues) to allow the propagation of high-frequency waves from the transducer to the sample [162] followed by a detection of the echo signal. In case of defects, the acoustic impedance (the product of sound density and speed) is modified and thus reflection and refraction of the ultrasonic waves is affected [163]. This method has the advantage of being non-destructive, hence the ion traps are still usable after the analysis of the interface. This helps finding explicitly well-bonded traps for the experiment.

We performed a CSAM analysis on both bond interfaces achieving a lateral spatial resolution of 10 µm. The signal emitted by the transducer is focused on the desired interface. While scanning across the whole wafer surface, the amplitude of the reflected signal is recorded. The recorded amplitude is then converted into a color code, to visually demonstrate the quality of the bond: Gray regions represent well-bonded areas, where the acoustic waves are not reflected at the interface, whereas at the positions of voids, a change in the acoustic impedance due to vacuum, air or water is visible through bright coloring. The CSAM analysis of one bottom bond between bottom and spacer wafer revealed a well-bonded area of 93 %, estimated by an evaluation of the recorded image. As visible in figure 5.23a, only a few voids close to the wafer edge are detected. The interface between the spacer and top wafer of the same ion trap wafer stack has a well-bonded area of 88 %, caused by voids mainly located in the outer area of the wafer surface. Because trap structures in the top wafer are only etched in the wafer center (black) where no reflection is detected, the same structures appear white at the wafer edge where the silicon is not etched.

Analysis of the depletion zone

Another tool to verify a successful wafer bond is an analysis of the width of the depletion zone formed in the glass during anodic wafer bonding, as described in section 5.2.4. One method of analyzing the depletion zone is to characterize an SEM cross section to visualize the different materials of the sample and to read out layer thicknesses. Therefore, a waferbonded ion trap chip was cut and polished to analyze the layer cross section by SEM. To simplify identification of the different layers, the sample was etched with 5 % HF for 20 s, resulting in a short etching of the surface, with varying etch rates for the different materials: the depletion layer with a lower content of sodium ions

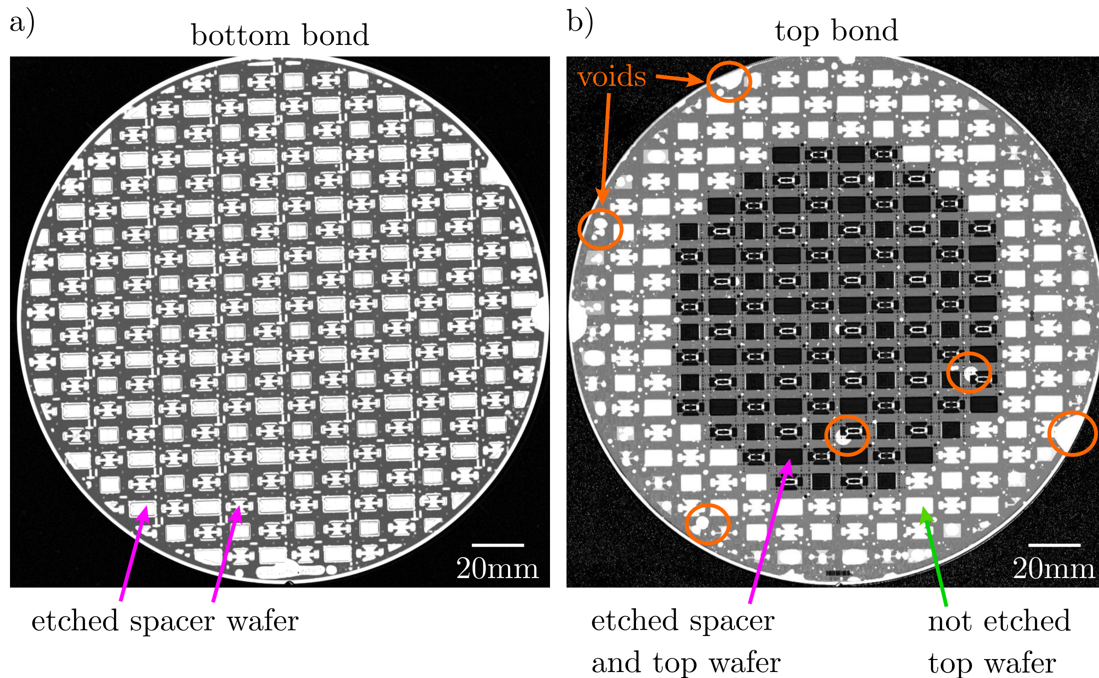

Figure 5.23: CSAM of the bottom (bottom and spacer wafer) and top (spacer and top wafer) interfaces of the anodically bonded ion trap. a) The bottom interface has a well-bonded area (gray) of 93 %. The acoustic waves are reflected in white areas, that occur at the positions where the spacer wafer is etched and when air is enclosed in voids. b) The well-bonded area of the top interface with 88 % is reduced by voids (orange circles) mainly in the area close to the wafer edge.

exhibits a faster etch rate compared to the glass substrate, visible through a darker area in the SEM image. A thin layer of anions adjoins the depletion zone in the glass, featuring a brighter color in the SEM due to a lower etch rate. The width of the depletion zone was measured to be 254 nm, consistent with similarly performed bonds found in literature [164]. The recorded SEM image depicting the depletion zone is shown in figure 5.24. Moreover, an SEM cross section can also be used to identify local delamination or voids in the interface.

Die-shear tests

For a quantitative analysis of the mechanical stability of the wafer bond, die-shear tests are a suitable method of testing the bond strength on multiple samples with reduced effort compared to SEM cross sections. The chip (die) is glued on a base plate, with the bond interface parallel to the plate. A so called chisel is guided towards the fixed

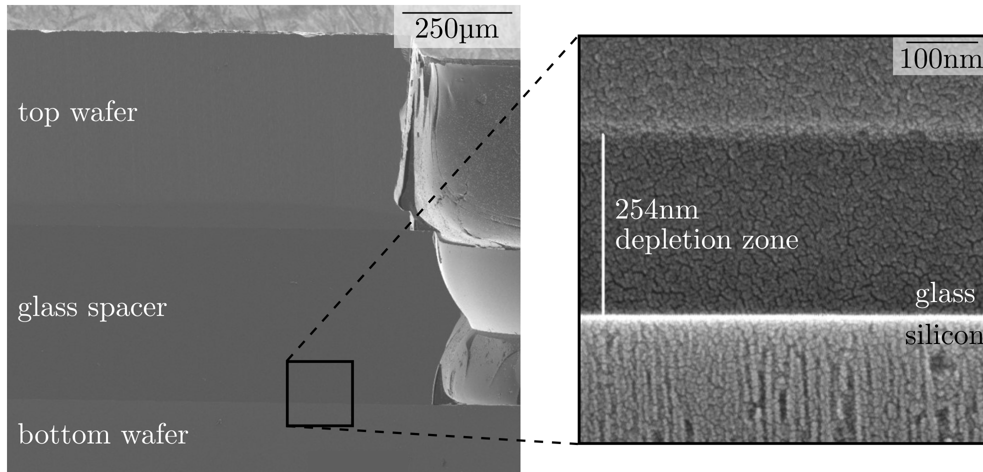

Figure 5.24: SEM image of the ion trap cross section with visible depletion zone formed during the anodic wafer bond. The left image shows the bonded triple stack formed by the bottom, spacer and top wafer. The zoom-in presented in the right image is a recording of the bond interface between bottom silicon and glass spacer. A decoration with 5 % HF for 20 s previous to the analysis leads to varying etch rates dependent on the material, to make the depletion zone with lower sodium ion content visible. The depletion zone (dark gray) has a width of 254 nm. The anion layer in the glass wafer adjoining the depletion layer can be distinguished through a brighter color.

sample. When in contact, the shear force F is increased until the die breaks and the shear strength is calculated by

$$\tau = \frac{F}{A} \tag{5.1}$$

with A the area the force is applied on. In addition, the bond strength can also be estimated via the observed failure mode: breakage along the interface indicates a weak bond; if cracks propagate through the material, the sealing between the two wafers is assumed strong compared to the material stability. The third scenario, in which the full chip detaches from the base plate, indicates a stronger bond compared to the adhesion of the glue.

Die-shear tests on 10 ion traps were performed to analyze the bond strength when using structured wafers. Because the ion trap chip has holes on every side for optical access, it is rather difficult to perform a reliable die-shear test on the assembled chip. The pressure to put on the sample is concentrated on a very small area compared to chip size and bonded area. Therefore, the ion trap chip was cut close to the center in

radial direction, so that only two of the four bonded glass pillars remained on the chip. For the test, the chisel was pushed towards the axial side of the chip, so that the chisel presses on both edges where the wafer is bonded. Because this method is difficult to apply to the structured ion trap chips, an analysis of the applied shear force is possible, but does not deliver meaningful results. The shear strength varies from $\tau = 9.5\,\mathrm{MPa}$ to $\tau = 19.3\,\mathrm{MPa}$ and is low compared to values found in literature with $\tau \approx 60\,\mathrm{MPa}$ [165]. However, all measured samples broke inside the material, indicating a well bonded interface. This demonstrates that the anodic wafer bond is a suitable basis to realize the hybrid ion trap. Details on the shear test are also given in Lina Purwins master thesis [159].

Cryo-cycling stress tests

Because the hybrid ion trap will be operated in a cryostat, the compatibility of the anodic wafer bond with a cryogenic environment was tested. Five ion trap chips were cooled down in liquid nitrogen followed by a warm-up to room-temperature. This test was repeated six times, to simulate the thermal stress applied in the real ion trap experiment. After each cryo-cycle, the chips were optically inspected for damage with a microscope. Every chip survived this test without any noticeable consequences or failures. Furthermore, three ion trap chips were cooled-down in a cryostat located at KAI several times, to achieve even lower temperatures of $\sim 17\,\mathrm{K}$. A following optical inspection revealed no visible damage, indicating a good compatibility with operation at cryogenic temperatures.

5.3.4 Detection and solving of failures

Prior to the experimental characterization of the ion trap, two issues occurred: first, a short between the two top electrodes was detected; second, a trap from the second batch broke during cool-down in the cryostat. This section describes the root-cause finding and solution to the observed failures.

Short between the top electrodes

When checking the ion trap for undesired connections between electrodes, a short in between the two top electrodes was observed. A connection due to wirebonds or defects could be excluded by performing measurements on multiple samples with and without wirebonds. An SEM image of the cross section of the trap at the position of the gaps separating the top electrodes shows some residual conductive silicon in the bottom of the gap, shorting the two electrodes. This issue was easily solved by increasing the

etching time of the DRIE. In figure 5.25, an SEM image of the layer cross section with and without short is depicted. When processing with increased etch time, also the substrate silicon below the buried oxide is slightly etched, as visible in the image. This does not affect the ion trap performance or mechanical stability.

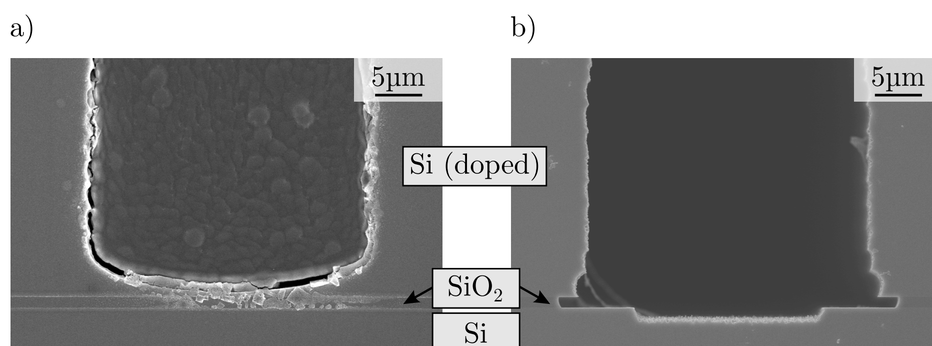

Figure 5.25: SEM images of the top wafer layer cross section. a) A short between the two top electrodes is visible due to residual conductive silicon in the gap. b) Cross section after increasing the etch time of the DRIE, resulting in well separated electrodes. Here, also the substrate silicon is slightly etched during the release etch.

Trap breakage in the cryostat

When cooling down one ion trap from the second fabrication batch, the chip broke inside the cryostat. Detailed inspections revealed, that cracks in the top wafer along the crystal axis (diagonal to the trap axis) led to a full detachment of parts of this layer. Where bonded to the glass spacer, the cracks run through the wafer and not through the bond interface, indicating a strong wafer bond in the interface between spacer and top wafer. A picture of the broken trap is shown in figure 5.26.

To find the root cause of the failure, different hypotheses were defined: stress caused by an newly integrated heater, increased stress caused by the Infineon carrier PCB and glue compared to the first batch of ion traps mounted on the ETH carrier PCB with softer glue, a weak wafer bond between bottom and spacer wafer, and a single event due to structural weakness. Therefore, shock-frost tests in liquid nitrogen were conducted with four traps from the same batch as the broken chips (referred to as second batch) as well as traps from the first batch. All traps from the second batch broke during this test. Moreover, mechanical stress tests of the mounted traps on the Infineon carrier PCB were performed on chips from the first batch that survived the thermal stress from the shock-frost experiment. When bending the PCB by external pressure to generate mechanical stress, the traps were not damaged. These tests indicate that neither the

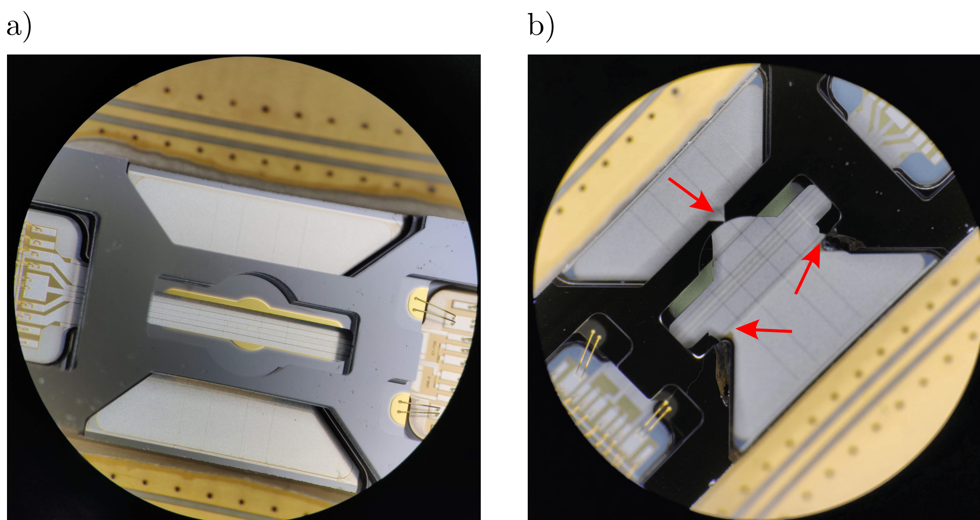

Figure 5.26: Hybrid trap broken during cool-down. a) One top electrode is completely broken out. b) The crack runs through the top wafer and glass spacer, not along the bond interface (see red arrows). This indicates a good wafer bond on the top bond interface, which can therefore be excluded as reason for the failure.

mounting on the Infineon carrier PCB, nor the additional heater are the root-cause for the failure. An analysis in the Infineon Failure Analysis department on one of the broken ion trap chips revealed a bad wafer bond of one spacer part to the bottom wafer, showing only a bond connection at the edge of the bond area. We expect a stress concentration on the small bonded area, when cooling down the ion trap, leading to cracks running through the whole wafer stack. From this point on, all further ion traps were tested for successful wafer bonding by CSAM analysis before being selected for operation in the experiment.

5.4 Ion trap performance

The hybrid trap was characterized in the laboratories of the TIQI (Trapped-Ion Quantum Information) group at ETH Zürich within the PIEDMONS collaboration. Incoming inspections and preparation of the ion traps were conducted by Chiara Decaroli, trap characterization and experiment operation were performed by Christopher Axline and Chiara Decaroli and reported in Chiara Decaroli's PhD thesis [45] and a published manuscript [141]. Although planned, participation in the on-site characterization of the author could not take place due to the regulations during the Covid-19 pandemic. Assistance and discussions were realized through remote correspondence.

5.4.1 Preparation and trap setup

Assembly of the ion trap was carried out at Infineon Technologies in Regensburg, as described in section 5.2.5. The hybrid trap was glued to a carrier PCB compatible with the ETH setup and subsequently wirebonded for electrical connectivity, as shown in figure 5.27. The traps were then shipped to ETH and prepared for the experiment.

Optical and electrical inspection

Upon arrival, the ion traps were optically inspected with an optical microscope and a SEM. Irregularities, visible defects and contaminations (such as the spots described in section 5.3.2) were detected during this phase. The traps with fewest defects and contaminations were selected to be inserted into the experiment chamber.

Before assembly in the cryostat, an electrical characterization was performed to detect potential shorts between electrodes, during which all electrodes were tested against each other. Within this testing process, a short between the two top electrodes was found in all the initial traps delivered to ETH. An analysis of the top wafer cross section at Infineon revealed residual conducting material in the gaps separating the two electrodes, as described in detail in section 5.3.4. Although the shorted electrodes limit the achievable tilt of the radial modes, they can be used in the experiment without further restrictions.

Trap setup

A detailed description of the setup which hosts the trap is given in [45]. The hybrid trap is mounted on the ETH carrier PCB made of Rogers 4350B. The carrier is connected to a DC filterboard using fuzz buttons made of gold[2]. The trap is surrounded by a gold-coated copper cage used as both a shield as well as a ground layer. The box has 8 openings for laser access and a transparent gold mesh attached on the top side. In figure 5.27a the trap setup is shown. At a later point, the trap setup was adapted to be compatible with the Infineon carrier PCB, as shown in figure 5.27b.

5.4.2 Trap characterization

After cooling down to temperatures around $6.5-7\,\mathrm{K}$ the first attempts to trap ions in the hybrid trap were performed using automated routines for loading ions, alignment of laser beams and the generation of voltage sets as described in [45]. An image of the first trapped ion after optimizing the imaging system is shown in figure 5.28. This section

[2] Fuzz Buttons®, Custom Interconnects

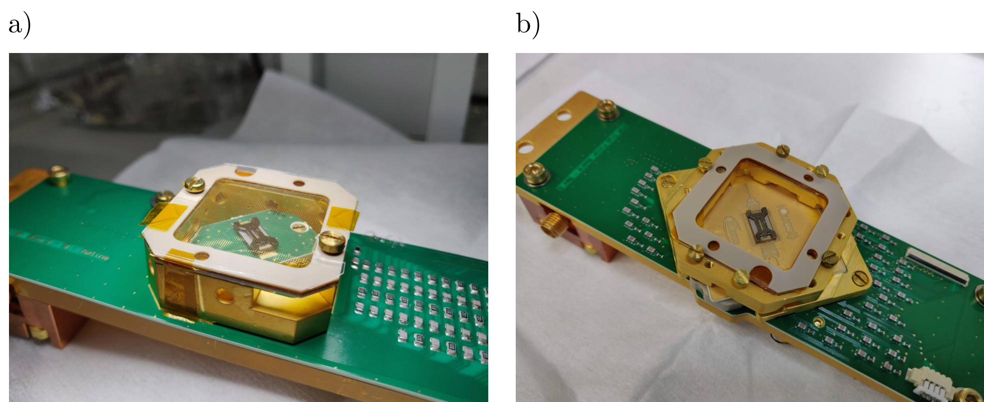

Figure 5.27: Trap setup used for the characterization of the hybrid trap in the experiment. a) The hybrid trap glued on the ETH carrier PCB and connected to the filterboard (green). A copper cage coated with gold and connected to ground is used as a shield layer against possible stray charges on nearby view ports. Openings on all sides allow for optical access. A transparent gold mesh creates grounding and shields from external stray electric fields. b) Adapted trap setup compatible with the Infineon carrier PCB (gold).

summarizes the results of the characterization of the first hybrid trap. Further details are given in Chiara Decaroli's PhD thesis [45].

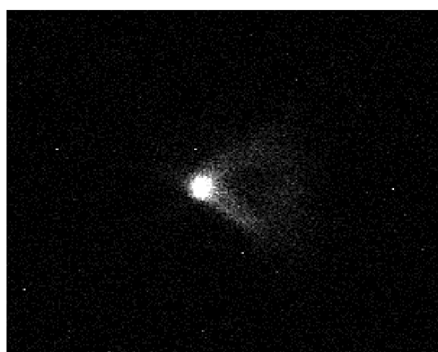

Figure 5.28: Image of the detected fluorescence indicating a trapped ion in the hybrid trap.

State preparation

In order to benchmark the operation of the trap, the ion was initially cooled and prepared in the desired ground state as a preparation for quantum operations. Using a state preparation technique with σ-polarized 397 nm laser light as described in section 2.4.3,

population was transferred from the $4S_{1/2}, m_j = +1/2$ to the $4S_{1/2}, m_j = -1/2$ state and Rabi oscillations between these two states were observed. The initial contrast of the oscillations was 70 %, see figure 5.29a. The limited contrast was traced to an additional oscillating magnetic field originating from the trap itself which decreased the overlap between the state preparation beam and the magnetic field direction. In figure 5.29b the suspected direction of the oscillating magnetic field is depicted. Based on findings from other experiments in the research group [166, 167] and from the characterization of the 2D twin trap (see section 4.5.3) the time-varying magnetic field is assumed to be caused by the high capacitance of the RF electrodes to the underlying ground plane of 52 pF. A reduction of the RF capacitance by using a wide-bandgap substrate material to bypass the need for a GND shield layer will mitigate the effects of oscillating magnetic fields on the trap performance.

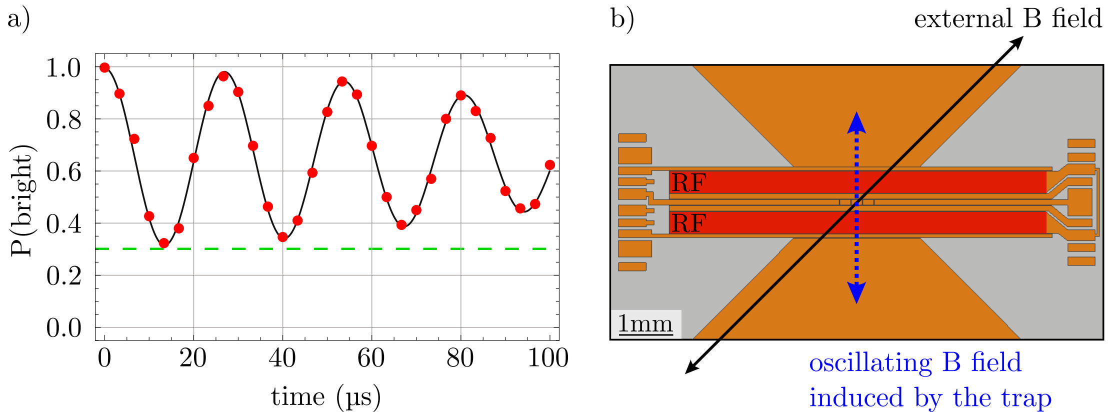

Figure 5.29: a) Rabi oscillations of the ion with a maximum contrast of only around 70 % (green dashed line) between bright and dark state. b) Suspected direction of the oscillating magnetic field (blue arrow) induced by the RF electrodes of the ion trap (red) with respect to the external magnetic field (black arrow). Figure adapted from [45].

Trap parameters and heating rate

The next step of the characterization routine is an analysis of the motional frequencies of the trapped ion. The measured radial frequencies of 2.600 MHz and 2.859 MHz and axial frequency of 1.484 MHz correspond to a trap depth of 0.3 eV in simulations.

As theoretically described in section 3.2.2, the heating rate of the hybrid trap was measured using the sideband ratio method. The best measured values were in the range of ∼40 q/s at cryogenic temperatures. The measured heating rate is comparable to

other state-of-the-art ion traps [92, 99] and allows for a stable operation of single ions as well as ion strings [141].

Stray electric fields

In order to perform reliable, high-fidelity quantum operations, the trapped ions should not be exposed to stray electric fields generating micromotion, which cannot be compensated for. When tuning the axial confinement of the trapped ion, a shift of the ion along the trap axis was observed. One possible explanation for this behavior are charge effects in the dielectrics that generate electric fields in axial direction. Since several laser beams pass the dielectric spacer sidewalls at a distance of only a few $10 - 100\,\mu m$, we suspect the presence of stray charges in the spacer dielectric caused by scattered laser light.

To verify this hypothesis, the ion position was shuttled along the trap axis by $\pm 200\,\mu m$ from the central trapping site. In several ion positions, micromotion compensation was performed. The stray field for the radial and the vertical plane is then calculated by using the required compensation voltages. In figure 5.30 the calculated stray fields in radial (x) and vertical (y) direction are shown. This analysis indicates a change in the stray field along the trap axis of a few hundred volts/meter within the shuttled ion position. While the observed static stray electric fields could be well compensated, a metal coating of the spacer sidewalls and a recess of the gap oxide between the trap electrodes could further help reducing the amount of stray electric fields originating from bulk dielectrics.

5.4.3 Discussion

We successfully designed, fabricated and characterized a new hybrid ion trap that is formed by a planar trap with enhanced trap depth thanks to additional top electrodes.

In the first iteration of the hybrid ion trap a short between the two top electrodes was observed. Therefore, it was not possible to put individual voltages on the two electrodes, resulting in a limited tilt of the motional modes and thus limited laser cooling. With voltage sets optimized for this condition, we were able to achieve a trap depth of 0.3 eV. The next iteration ion traps with isolated top electrodes provide more flexibility in the applied DC voltage sets and thus a trap depth aligned with the targeted 1 eV should be possible. Moreover, after finishing the trap characterization of the first hybrid ion trap, an additional heating element was integrated into the trap setup. The heating element is in direct contact with the carrier PCB, allowing for a measurement of the heating rate dependent on the trap temperature. This allows one to determine the correlation

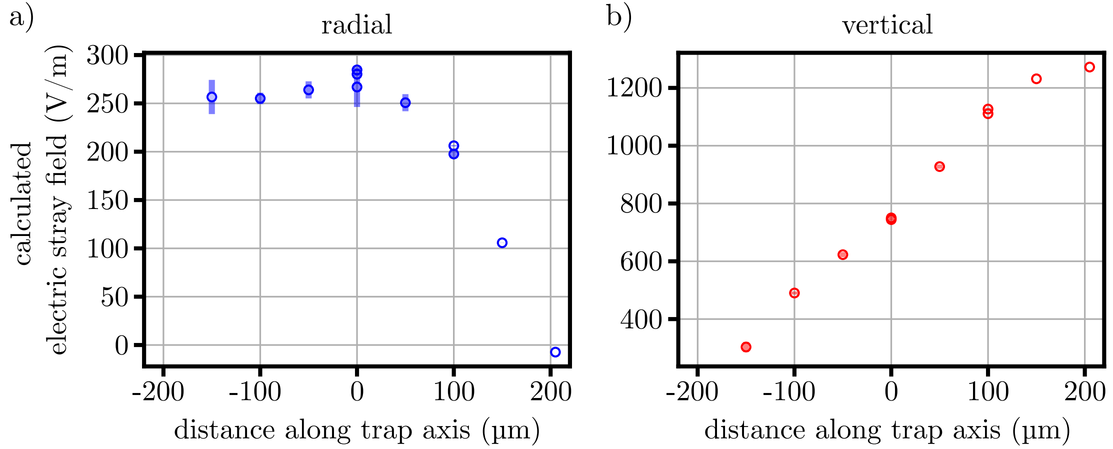

Figure 5.30: Calculated stray fields derived from the applied compensation voltages in a) radial and b) vertical direction. The stray field in vertical direction gives much higher values compared to the in-plane stray field. Error bars are partially hidden by the displayed data points. Figure adapted from [45].

between heating rate and temperature, and thus helps to extract the room-temperature heating rate.

While characterizing the ion trap properties, we observed two limitations: i) the relatively high trap capacitance of 52 pF of the RF electrodes leads to an oscillating magnetic field perpendicular to the external magnetic field, and ii) stray charges generate additional micromotion of the ion. A solution to the first problem is either a reduction of the parasitic capacitance by changing the layout and materials used for the ion trap, or decreasing the RF amplitude (resulting in a lower trap depth). In the current design, an oxide layer of 4.4 µm separates the RF electrodes in the metal 3 layer from the ground shield in the metal 1 layer. Changing the material separating the metal layers to one with a lower permittivity such as SiOF or SiCOH [168] helps reducing dielectric losses. On the other hand, changing the substrate material to one with a wide band gap such as fused silica or sapphire allows for omitting the ground layer necessary for silicon substrates. This significantly reduces parasitic capacitance of the RF electrodes. As a second point ii), stray electric fields are observed in the ion trap, which we suspect are originating from unshielded dielectrics. Despite the relatively large distance of >1.5 mm of the glass spacer to the trapped ion, the effects of stray charges in the dielectric are not negligible. A metal coating of the glass sidewalls and the possibility to bias the surface should significantly reduce the occurrence and consequences of stray charges in the dielectric. Moreover, if the openings for laser access are created with an anisotropic

etch or laser cutting, the spike in the glass is avoided. This would lead to another ~85 µm larger distance of the laser to the spacer sidewalls and avoids concentrated field lines at the position of the spike. Thus, the amount of scattered stray light on the surface is reduced, without the need to decrease the wafer bond area that connects the three layers. dielectrics in the gaps between electrodes could be reduced by an isotropic underetch of the electrodes, as described in section 4.2.3.

Chapter 6

Proposal for a 3D ion trap array

The contents of this chapter are also included in the Patent submitted to the EPA with official application file reference 22183532.5 on 7th July 2022.

In the previous chapters two microstructured ion trap prototypes have been presented: a surface trap with 2D array geometry and a linear surface trap with enhanced confinement facilitated by electrodes in an opposing top layer above the bottom electrodes. The next step towards a scalable, microstructured ion trap is to combine the 2D array geometry of the 2D twin trap with the three-dimensional architecture of the hybrid trap to ensure stable trapping of a large number of ions in a trap array. In this chapter, a concept for such an ion trap is presented. The geometric layout of the new proposed trap concept is based on a scaled array structure consisting of parallel linear arrays and makes use of the increased confinement potential of a three-dimensional architecture. A strong confinement of the ions in the trap is an important prerequisite for successful ion shuttling in the trap without ion loss. Microfabrication of the proposed ion trap is possible with industrial micro-electro-mechanical systems (MEMS) fabrication techniques, and includes multiple metal layers, dielectric substrates and wafer bonding to connect the single wafers forming the 3D architecture. Basic simulations of the trap concept were performed, and achievable secular frequencies, trap depth and required DC and RF voltages are presented. Moreover, proposals on how to address the main fabrication challenges are given.

6.1 Trap concept

The goal of the presented trap concept is a microstructured ion trap with 2D array geometry, which provides a sufficiently deep confinement potential to avoid ion loss and thus enable a stable trap operation as basis for quantum information processing.

Therefore, the geometry of the 2D twin trap is adapted and extended by a top layer and spacer, as already introduced with the hybrid trap. For the trap concept, the characterization results of both the 2D twin trap and the hybrid trap are taken into account. One main issue of both traps is the RF capacitance of around 1.9 pF normalized to one trapping site, which would limit practical implementations to few tens of ions. We suggest using a wide-bandgap material as wafer substrate to circumvent the need for a shield layer: i) wide-bandgap materials have a low loss-tangent and thus heat dissipation into the substrate can be reduced, and ii) stray charges in the substrate caused by stray light can be significantly decreased. In a substrate material with a bandgap larger 3.3 eV none of the lasers used in the experiment are able to induce charge carriers [124]. This energy value corresponds to the highest-energy laser light with 377 nm wavelength used for photoionization during trap operation. However, using a wide-bandgap material such as fused silica or sapphire prevents the integration of electronics directly in the substrate, which might be important when scaling to hundreds of trapped ions and thus increasing the number of DC electrodes to a similar range of hundreds of electrodes. Separating RF and DC electrodes to two layers, namely a wide-bandgap substrate for the RF electrodes and a silicon substrate for the trap's DC electrodes, might enable an ion trap capable of integrated electronics such as digital-to-analog converters (DACs), switches or filters while at the same time avoiding high capacitances induced by the trap's RF electrodes.

A proposed trap design is shown in figure 6.1. The bottom layer includes all DC electrodes used for axial confinement and shim electrodes to compensate for stray electric fields. The top layer provides the RF electrodes for radial confinement. The two layers are separated by a spacer, defining the distance between bottom (DC) and top (RF) electrodes.

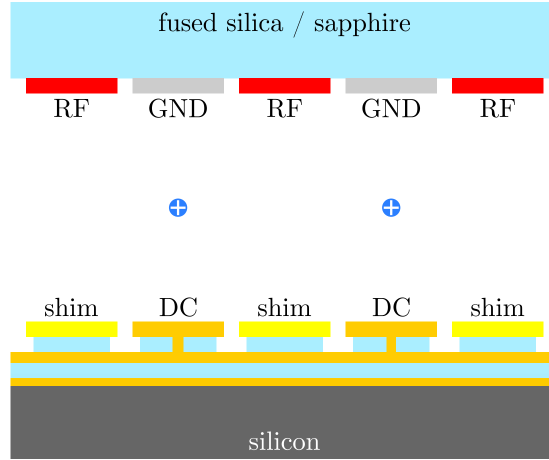

Figure 6.1: Schematic cross section of a scalable ion trap with separated DC and RF electrodes in two layers to trap ions (blue circles) in a 3D architecture. A silicon bottom wafer (dark gray) provides DC (orange) and shim (yellow) electrodes, whereas the RF electrodes (red) are implemented on the top layer (light blue) made of fused silica or sapphire. The RF electrodes are alternated with GND electrodes (gray).

6.2 Design challenges

In this section, we discuss the main challenges in the proposed ion trap concept and how to address them:

- **RF capacitance**
  In both the 2D twin trap and the hybrid trap the RF electrodes form a capacitance with DC and GND electrodes of 44 pF and 53 pF, respectively. A high capacitance leads to an increased power dissipation in the trap, reducing the RF voltage gain via the step-up resonator and at the same time heating up the ion trap. As described in section 5.3 a high trap capacitance can also cause shifts of the qubit frequency due to a time-varying magnetic field. In both traps discussed in this thesis the main contribution to the trap capacitance is formed between RF electrodes and the GND shield electrode in the lowest metal layer, as shown in figure 6.2.

  When scaling to a larger number of trapping sites, also the number of RF electrodes increases, thus raising the trap capacitance. One approach to reduce RF capacitances in ion traps is using a wide-bandgap material substrate, which does not require shielding as discussed above. However, when realizing complex trap

layouts as surface traps, multiple metal layers are necessary and a crossing of DC leads and RF electrodes in superimposed layers can often not be avoided. In the 2D twin trap, the innermost DC island electrodes can only be connected to the bonding pads by crossing the RF electrodes in a lower metal layer. To avoid RF pickup on these DC electrodes, an additional GND layer between the RF electrode in the top metal layer and the DC electrodes is integrated in the intermediate metal layer, which contributes to the RF capacitance. Note, that RF pickup induces an RF voltage component of the DC electrodes, which can not be compensated for. Therefore, the GND shield layer cannot be omitted.

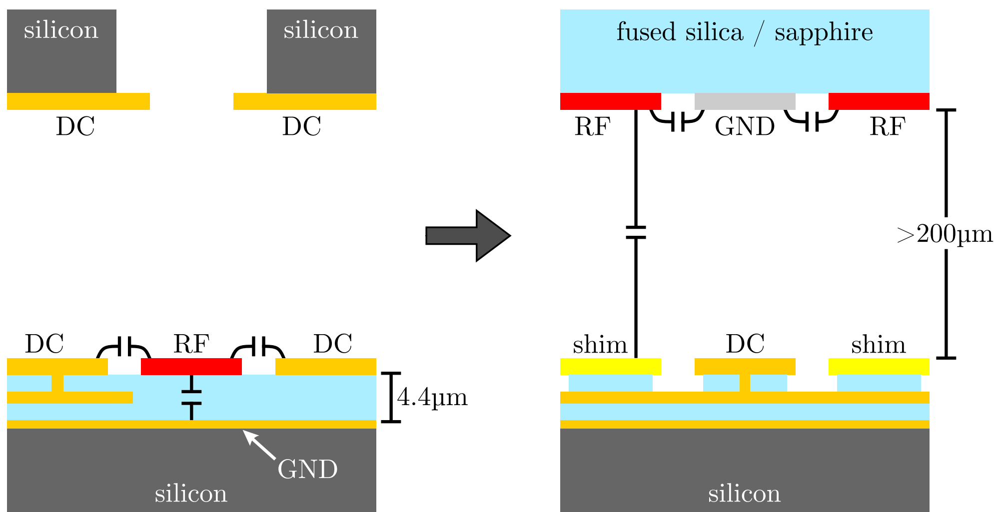

Figure 6.2: Schematic representation of the ion trap. The capacitance between RF and DC/GND electrodes in typical surface trap designs (left) can be reduced by separating RF and DC electrodes on two different wafers (right).

The proposed trap design is based on a vertical separation of DC and RF electrodes: The RF electrodes are placed on a separate wafer with only one metal layer, based on a wide-bandgap material. Thus, there is no need for a shield layer set to GND, reducing the trap capacitance significantly. To determine the reduction of trap capacitance in such an ion trap design, a simulation was performed. In this simulation, the layout including the full layer stack of the 2D twin trap was compared to the layout of the 2D twin trap on wide-bandgap substrate, and the 2D twin trap with separated DC/RF electrodes in a 3D architecture. Note the layout differences of the silicon 2D twin trap and the wide-bandgap 2D twin trap: while the silicon trap has a large GND layer in the lowest metal layer and only one crossing of DC and RF lines in the trap center, the wide-bandgap trap has

no GND shielding layer, but a total of three areas of RF and DC crossing due to some design changes as will be described in [120].

Using a wide-bandgap substrate material decreases the total trap capacitance from 1.9 pF to around 1.2 pF normalized to one trapping site, increasing linearly when scaling up to 1000 trapping sites. Additional layout optimizations would be necessary in order to exploit the full potential of this approach. Separating DC and RF electrodes compared to a surface trap on wide-bandgap material additionally reduces the trap capacitance around 1-2 orders of magnitude, resulting in a capacitance of $20 - 100$ pF for a 1000-trapping-site trap design, compared to 1.2 nF for the wide-bandgap 2D twin trap.

- **Stray electric fields**
  The presence of stray electric fields in an ion trap can lead to excess micromotion of the ions. Stray charges can be generated by stray light on the trap surface and can reside on any non-conductive surface. In the presented ion trap design, the silicon bottom wafer needs to be shielded by a continuous GND plane to avoid light-induced stray charges in the silicon substrate generated by accumulation and inversion [108], and to reduce dissipated energy from the RF electrode to the substrate. The metal layers are separated by inter-metal oxide, which fills the gaps in between the electrodes. An isotropic etch of this oxide down to the underlying GND plane leads to a recess of the oxide below the electrodes, as visible in figure 6.3. Thus, the influence of stray charges in the oxide can be significantly reduced due to a better shielding of the surrounding metal layers.

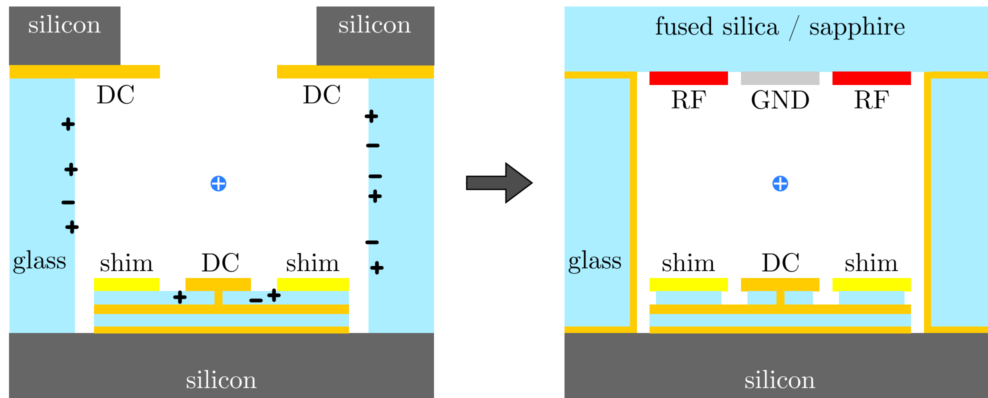

Figure 6.3: Schematic representation of the ion trap. The effect of stray charges in the gap oxide between electrodes and on the glass spacer sidewalls (left) can be reduced by isotropically etching the gap oxide and a metallic coating of the spacer sidewalls, respectively (right).

Moreover, coating the glass spacer separating the top and bottom wafer with a metal layer (e.g. Au or ITO) allows for connecting to GND to reduce the amount of stray charges on the dielectric spacer sidewalls. The metallization could be done by an evaporation of an adhesion layer (e.g. Ti) followed by evaporation of the desired metal. If the thickness of the metal coating is only a few tens of nanometers [169, 170], the material is transparent enough for a suitable combination with integrated waveguides.

- **Compensation electrodes**
  When scaling the 2D twin trap beyond one hundred trapping sites, a basic geometry can be realized by alternating a rail of segmented DC electrodes with an RF rail. However, this geometry does not allow for proper operation as a quantum processor, because it lacks DC shim electrodes necessary to compensate for stray electric fields, as shown in figure 6.4.

  When scaling to a larger number of trapping sites, especially when extending the layout in the radial direction where RF and DC rails are alternated, additional space for compensation electrodes (shim electrodes) needs to be created. A trap design with separated RF and DC electrodes enables the integration of compensation electrodes at the position of the RF electrodes in the surface trap, which are now moved to the top layer.

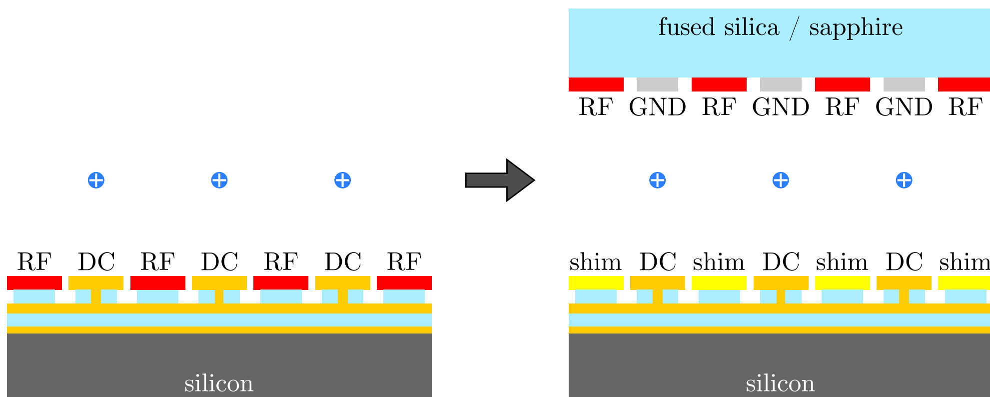

Figure 6.4: Schematic representation of the ion trap. When the ion trap layout with 2D array architecture is scaled up, there is not enough space for shim electrodes (left). Moving the RF electrodes to an additional top layer allows for the placement of shim electrodes between the DC electrodes on the bottom layer.

- **Routing**

  With a growing number of trap electrodes also the number of electric leads on the trap chip increases. The size of these leads should not be chosen too small, as with an increasing resistance Johnson-Nyquist noise is induced, causing motional heating of the ions, see section 3.2.1. Typical lead lengths of 5 mm, a lead width of $10 - 20$ µm (dependent on the size of the electrodes that scales with the ion-surface distance) and a common routing layer thickness of 1 µm gives a resistance of a few Ohms per lead at room-temperature, resulting in a heating rate caused by Johnson noise of a few quanta per second. Operation at cryogenic temperatures leads to a decrease of the resistivity of AlSiCu with a factor of around 10 and a reduction of the heating rate of around two orders of magnitude, as discussed in section 4.3.1. For this reason, the size of leads should not be reduced, and the concept for connecting all electrodes to the carrier PCB should be carefully elaborated.

  There are two approaches to solve the issue of lacking space for suitable DC leads: i) implementing additional metal layers to distribute the routing over several levels, and ii) using through-substrate vias (TSVs) [35, 171] to connect (some of) the electrodes directly to the carrier printed circuit board (PCB) below the trap chip. The ion traps presented in this thesis are both based on a silicon substrate, on which three metal layers are deposited. In general, the used technology is expandable to up to five metal layers to provide the routing of electric leads, where the lowest metal layer should be a GND plane to shield the substrate. However, with five metal layers and the corresponding isolating inter-metal oxide layers, the topology of the trap chip increases significantly, reaching values of ≥ 10 µm dependent on the exact trap layout. Therefore, planarization steps have to be included to the process flow, such as chemical-mechanical polishing (CMP) [105], to ensure a reliable fabrication with optical lithography.

  In the top wafer, only three electrodes are necessary: two alternating RF electrodes separated by GND electrodes, as shown in figure 6.5. Simulations have shown, that biasing the GND electrodes improves trap depth. One method for electrical connection of the electrodes to the carrier PCB is using through-glass vias (TGVs) from the top to the bottom layer. On the bottom layer the leads are routed either to the bonding pads on the trap chip or directly to the carrier PCB using TSVs. Another possible approach to connect the RF and GND electrodes to the bottom layer is to use a metal-coated spacer and a eutectic waferbond, as sketched in figure 6.6. Here, every spacer part could route one electrode, therefore at least three separate glass blocks are necessary to realize this approach.

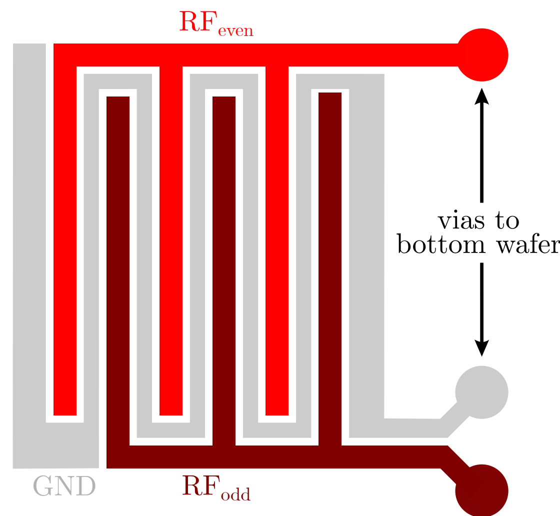

Figure 6.5: Schematic routing of the RF electrodes on the top wafer in a single metal layer. Two separate RF voltages are applied to the RF electrodes $\mathrm{RF_{even}}$ (light red) and $\mathrm{RF_{odd}}$ (dark red). The electrodes sharing the same voltage are connected on one side of the chip and electrical contact is achieved via TSVs to the bottom wafer and further wirebonding to the carrier PCB. In between the RF electrodes, a GND electrode (gray) is integrated.

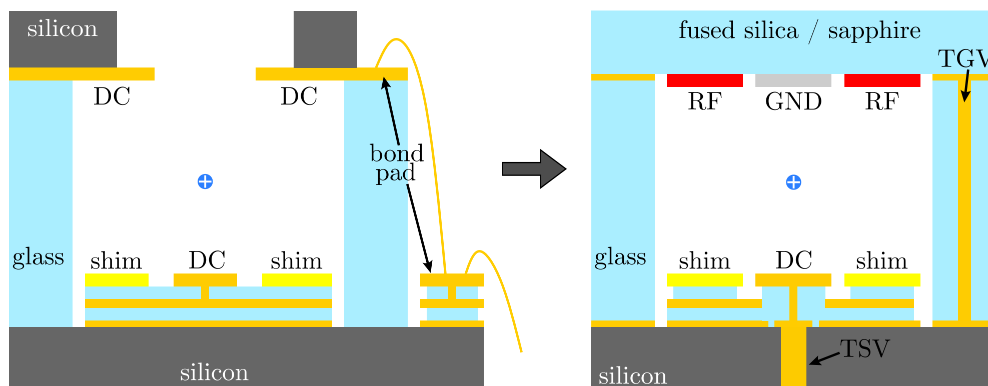

Figure 6.6: Schematic representation of the ion trap. Using only wirebonds to connect the trap electrodes to the carrier PCB (left) becomes more difficult when scaling the ion trap due to a lack of space for bond pads. This issue can be solved by using TGVs to connect the electrodes on the top wafer to the bottom layer and TSVs to realize connections to the carrier PCB below the trap chip.

- **Laser addressing**
  Optical access in microstructured 3D ion traps is often limited by bulk electrodes, substrates and spacer parts. When scaling to a large number of ions positioned in a 2D array geometry, the chip area containing electrodes, which form the trapping sites, increases linearly. This area has to be fully accessible to laser light. However, laser access into the vacuum chamber or cryostat is often limited when using free-space optics. Using a glass wafer as a spacer between top and bottom layers allows for integrating optical waveguides to allow the precise addressing of ions in the trap, as visualized in figure 6.7.

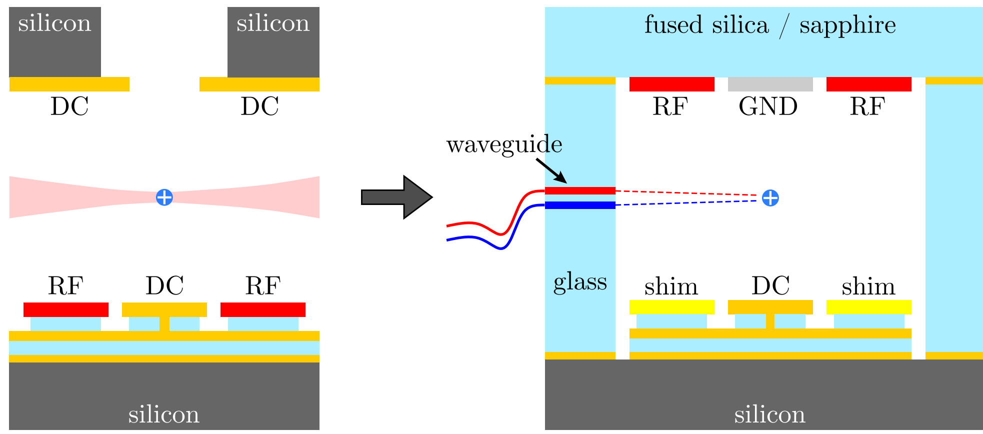

Figure 6.7: Schematic representation of the ion trap. The need of free-space optics (left) to address single trapped ions can be avoided by integrating optical waveguides in the glass spacer (right).

Using femtosecond laser micromachining, single-mode waveguides can be written directly in crystalline dielectrics [172–175]. These waveguides can include curves to reduce stray light and allow for complex array structures. However, total losses given by incoupling, propagation and outcoupling loss are typically in the range of a few decibels per centimeter, dependent on wavelength and substrate material. The integration of waveguides for infrared light with 729 nm wavelength into sapphire for ion traps has already been investigated [176]. The fabrication of waveguides for blue light such as the laser cooling and state detection laser with 397 nm wavelength used in this thesis is challenging, as propagation losses increase at smaller wavelengths [177]. Additional lasers for ionization, cooling and repumping can be implemented as global laser beams to simultaneously address multiple trapping sites.

- **State detection**
  One challenge of the microfabricated 3D trap is sufficient optical access to collect photons for state detection of the ions. As we have seen in simulations, biased GND electrodes in between the RF electrodes on the top wafer are necessary to achieve a suitable confinement potential. Although there is in principle enough space for these electrodes, if one wants to detect the ion's fluorescence from top (as this is the only option for ion-specific state detection in a 2D array architecture), massive electrodes prevent the photons to pass through the transparent top wafer. However, if using a transparent metal coating such as ITO (indium tin oxide) [178–180] on the glass wafer to form the GND electrodes, a high proportion of the photons is transmitted. A possible implementation of state detection through a transparent substrate by using ITO as conductive material to form GND electrodes is shown in figure 6.8.

  ITO has a resistivity of $\rho \approx 1 \times 10^{-6}\,\Omega\,\mathrm{m}$ [181], which is around two orders of magnitude higher than the resistivity of the AlSiCu alloy used as electrode metal in the ion traps presented in this thesis, see section 4.3.1. Thus, it should not be used as preferred metal to form the RF electrodes of the ion trap to avoid increased heating. Another possibility for state detection is using integrated optics such as lenses to collect the photons directly on chip [146, 182].

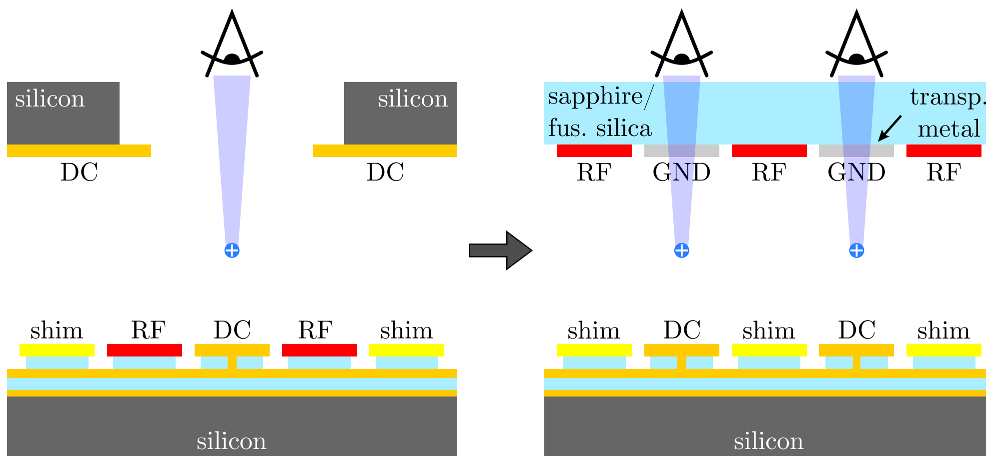

Figure 6.8: Schematic representation of the ion trap. In the hybrid trap, a slit in the silicon topwafer is needed for state detection (left), whereas in the proposed ion trap design, camera access from top is achieved by using a transparent metal to form the electrodes on the top wafer.

6.3 Simulations

A scalable design for several hundred ions with individual control requires complex trap designs including multiple RF and several hundreds of DC electrodes. Besides the before mentioned issues of a lacking space for compensation electrodes and a strongly increasing coupling capacitance between RF electrodes and the adjacent DC electrodes, additional operational difficulties arise when scaling the number of electrodes: i) the RF voltage amplitude needs to be increased to maintain a decently high confinement potential to trap the ions [79], and ii) with a growing number of trapping sites the trap depth decreases, so that stable operation of the ions as qubits can no longer be guaranteed if the RF voltage is not increased. To solve this problem, a three-dimensional architecture can be used that allows for a higher confinement and thereby eliminates the need for impractically high RF voltages for reliable trap operation.

To investigate the effects of the proposed trap concept with separated RF and DC electrodes, we conducted simulations[1] of an ion trap with basic geometry including RF rails on a top wafer and DC/GND electrodes on a bottom wafer, and extracted the most important trap parameters as secular frequencies, voltage amplitudes and trap depth.

In the simulation, the wafers have a distance of 300 µm, RF rails have a width of 200 µm, and DC segments a width and length of 100 µm. A simplified version of the trap geometry for an 4x4 array layout is depicted in figure 6.9. In the following, the periodically connected DC electrodes forming a 1D array structure are referred to as DC rail. The RF voltage was optimized to achieve a stability q-factor of $q = 0.4$ at an RF drive frequency of 23 MHz. Figure 6.10 shows the simulated values for secular frequencies, RF/DC voltage amplitude and trap depth dependent on the number of parallel DC rails. In each DC rail, 10 trapping sites are located. For up to 25 parallel DC rails secular frequencies of ~ 0.8 MHz in axial and ~ 3 MHz in radial directions can be realized. These values are achieved with DC voltage amplitudes around 10 V and RF voltage amplitudes < 100 V. Moreover, when increasing the number of DC rails, the trap depth stays above 40 meV. This trap depth is much higher than the average kinetic energy of background gas molecules, which prevents ion loss due to collisions.

For a realistic trap design, the parallel RF rails can have two alternating widths to achieve a tilt of the radial modes that allows for laser cooling of all motional modes

[1] Simulations were performed in python using the *electrode package* developed by R. Jördens (https://github.com/nist-ionstorage/electrode). Although this simulation software is designed to study surface ion traps, an additional GND plane can be inserted as a counter electrode to compress the electric field. This allows the electric field generated by the RF electrodes to be simulated, rotated and shifted to the position of the counter electrode before summing the electric fields of all electrodes to obtain the total potential.

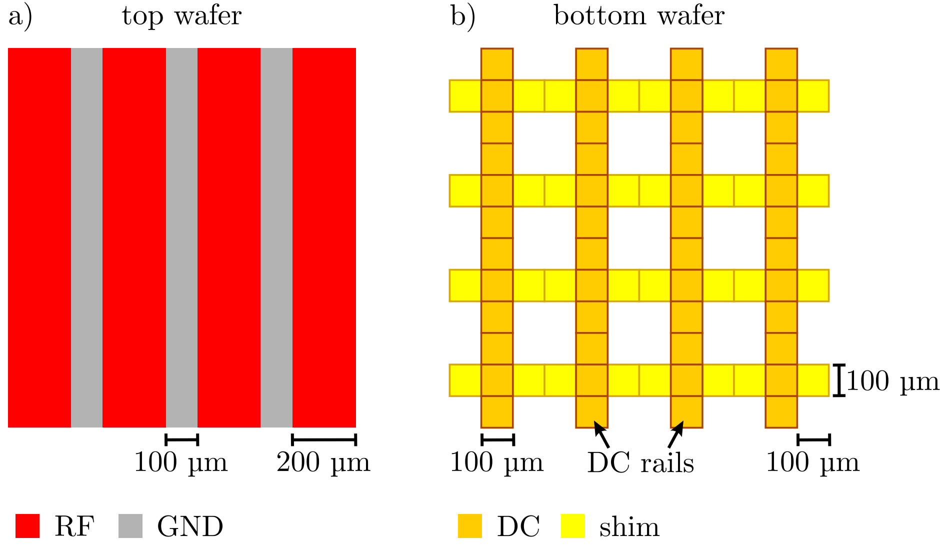

Figure 6.9: Simplified electrode layout and dimensions used for the simulation of the proposed 3D trap array with 4x4 trapping sites. a) Top wafer geometry with RF (red) and GND (gray) electrodes. b) Bottom wafer geometry with DC (orange) and shim (yellow) electrodes. Every third DC electrode is periodically connected. In the assembled trap, RF electrodes are positioned above the shim electrodes at a distance of 300 µm.

simultaneously. An optimization of the RF electrode widths is needed to enable RF coupling. Moreover, dummy electrodes next to the outermost trapping sites in both the axial and radial direction can be added to reduce edge effects. For coupling in axial direction along the DC multi-well, an additional segmentation of the DC electrodes would be necessary. This segmentation can be realized in the proposed ion trap design by using multiple metal layers for routing. In addition, a detailed analysis of the multi-well potential should be carried out in order to identify possible coupling in both axial and radial direction. Nevertheless, the preliminary simulation results predict suitable operating parameters for the presented trap concept, providing a scalable technology for future three-dimensional, microfabricated ion traps.

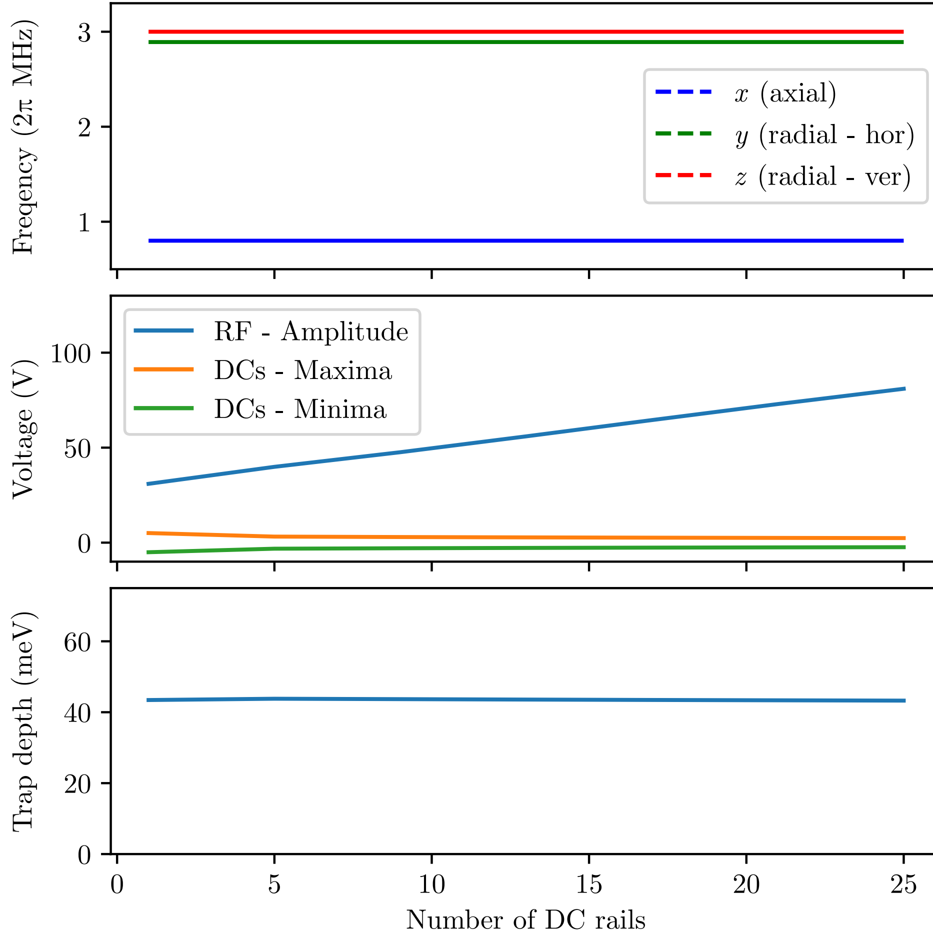

Figure 6.10: Simulated secular frequencies (top), voltage amplitude (center) and trap depth (bottom) dependent on the number of trapping sites for a trap architecture with separated RF and DC electrodes on two layers. Even for a large number of parallel DC rails, the RF voltage amplitude stays below 100 V and the corresponding trap depth stays above 40 meV enabling a stable operation as quantum processor.

6.4 Implementation and fabrication challenges

To realize the presented ion trap concept, the technology of the 2D twin trap and the hybrid trap can be adopted and needs to be expanded for TGVs, TSVs and integrated waveguides. In addition, the waferbond process must be adapted to the new wafer stack. In figure 6.11 a cross section of two alternative trap design with integrated functionality are sketched.

- **Through-glass vias**
  To create an electrical connection through a glass wafer such as borosilicate, fused silica or sapphire, metal-filled TGVs can be used [183–185] An interesting technology for the production of TGVs in thicker glass layers $\geq 300\,\mu$m is the laser-induced deep etching (LIDE) process [186]. Here, the glass wafer is irradiated with a picosecond laser in the area where the TGV should be formed. The irradiation leads to a local, permanent modification of the glass due to the interaction of the laser radiation with the processed material [187]. This allows for a selective etching of the modified material with hydroflouric acid. The TGVs are then filled with metal, e.g. copper or gold, to establish electrical contact. Typically, an adhesion layer (e.g. Ti) is deposited first, followed by a seed layer for electroplating of the desired metal to fully fill the TGV [184]. This process is compatible with an industrial production and thus could be an important component to realize a scalable trapped-ion quantum processor based on multiple electrode layers.

- **Through-substrate vias**
  TSVs are already widely used in MEMS technologies, since they can be combined with CMOS processing circuits, and at the same time reduce chip size while maintaining high performance [171]. In the field of ion traps, TSVs have been realized by Guise et.al. [35], where a ring-shaped hole was etched via deep reactive ion etching (DRIE) in a silicon substrate. After thermal oxidation of the silicon to create an isolation layer to the substrate, the hole is filled with $6\,\mu$m of highly p-doped polysilicon to generate a conductive connection. Here, the outer diameter of the TSV was $48\,\mu$m for a $300\,\mu$m thick substrate, which is in general small enough to enable TSVs for several DC electrodes on a trap with dimensions similar to the 2D twin trap and hybrid trap presented in this thesis. Furthermore, the integration of copper-filled TSVs in a silicon substrate connecting the trap electrodes to a glass interposer below the trap was used to realize a scalable surface ion trap by Zhao et.al. [188]. This trap was manufactured on 12” wafers, thus demonstrating the compatibility of TSVs with industrial production based on CMOS technology for ion traps.

- **Integrated waveguides**
  Regardless of the architecture used to scale the ion trap (2D ion trap array or QCCD architecture), the number of trapping sites or independent functional zones increases with the number of ions. This poses significant challenges for addressing individual ions with free-space optics, since a large area of the trap chip needs to be reached with all lasers at suitable beam angles without creating

cross talk between neighboring ions. Recently developed surface ion traps include lithographically structured optical waveguides in the trap substrate made of silicon nitride (SiN) and grating couplers to guide the laser light towards the trapped ions [39, 189]. The integration of waveguides into the trap substrate create a reliable hardware that bypasses the need for laser beam alignment and can reduce noise and drifts when performing quantum logic operations. An alternative technology to include light-guiding in three-dimensional ion traps is given by laser-written optical waveguides in dielectric materials as fused silica or sapphire [176]. Femtosecond laser pulses are used to locally modify the crystal lattice of a transparent material, leading to a decreased refractive index in this area due to amorphization [172]. By changing the focus position of the laser, it is possible to create three-dimensional structures such as curved waveguides to allow for controlled light guiding.

- **Waferbond process**
  To assemble the individual wafers of the ion trap into a 3D architecture, they are joined by wafer bonding. Using a eutectic wafer bond allows for connecting a top and bottom wafer electrically. TGVs filled with metal can be used to route the RF and GND electrodes from the top to the bottom wafer and to the bonding pads for electrical connection to the carrier PCB by wirebonding. However, the coefficient of thermal expansion (CTE) must be taken into account when choosing the substrate materials, to avoid wafer breakage during the wafer bond process at higher temperatures of $\geq 300\,^{\circ}\mathrm{C}$ and when cooling down to room-temperature or even cryogenic temperatures for trap operation. Common substrate materials for waferstacking in MEMS technologies are silicon and borosilicate glass, which are CTE matched in a wide temperature range [190]. The compatibility of a waferbond formed by these substrates with ion traps has already been demonstrated by the hybrid trap presented in this thesis for operation at room temperature and at cryogenic temperatures [141]. While direct waferbonding of two fused silica wafers was successfully performed [191], a waferbond of fused silica or sapphire to borosilicate glass as proposed in the presented ion trap concept is still to be investigated.

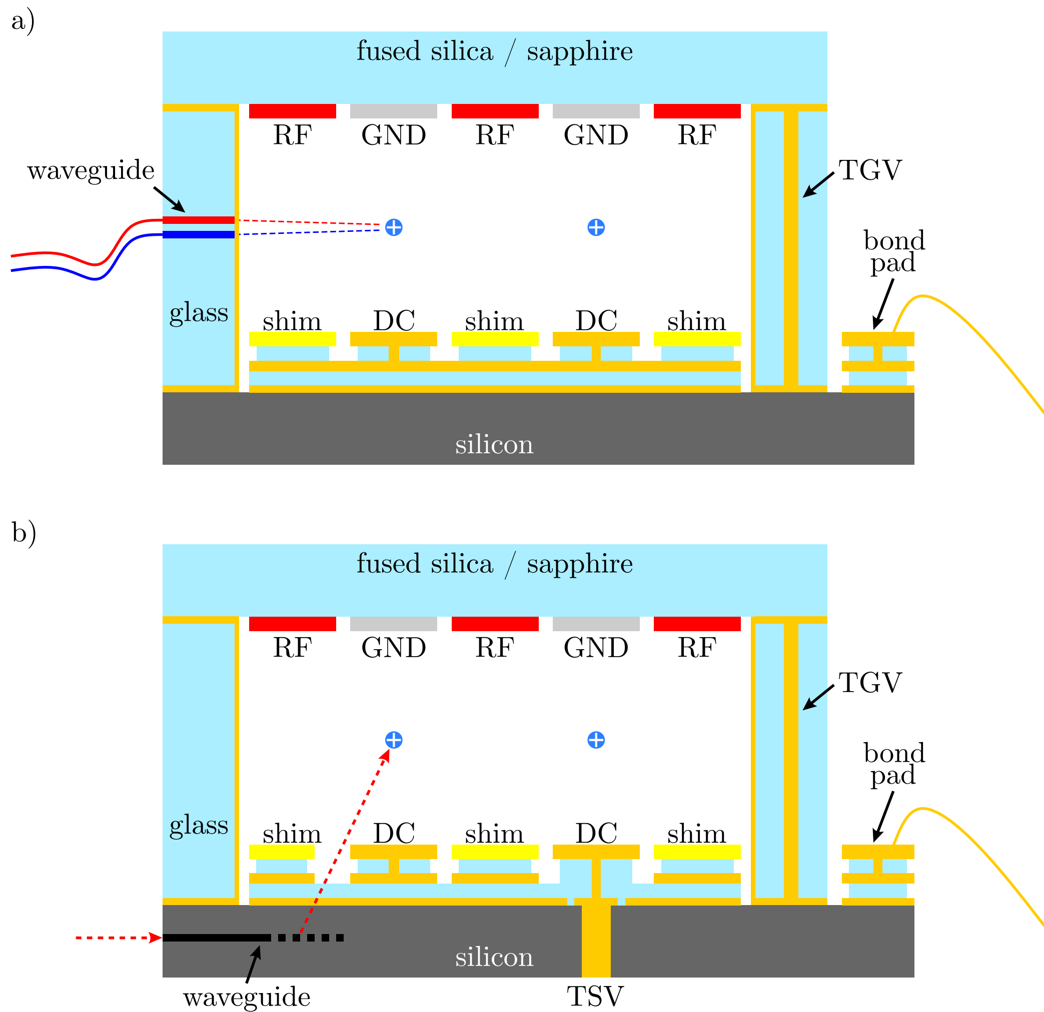

Figure 6.11: Schematic cross section of the ion trap shown in figure 6.1. a) Design with integrated waveguides in the glass spacer (light blue) and TGVs to connect top (light blue) and bottom wafer (dark gray). Electrical connection to a carrier PCB can be achieved by wirebonding to bond pads on the bottom wafer. b) Alternative design with integrated waveguides in the bottom wafer (light blue) and TSVs to connect electrodes directly to the chip carrier through the silicon substrate.

6.5 Outlook

At the time of writing this thesis, several projects are ongoing on the development of different aspects of the proposed scalable 3D ion trap concept:

i) Isolating substrates (such as fused silica and sapphire) are currently investigated to serve as substrate material for future ion traps with multiple metal layers to create and route segmented electrodes without the need to integrate a shield layer. This reduces the trap capacitance significantly.

ii) The OptoQuant project [192] focuses on the integration of optical waveguides for red and blue laser light in the spacer wafer made of fused silica or borosilicate glass. Waveguides are written into the substrate by femtosecond laser pulses with an alignment accuracy in the sub-micrometer range, which is crucial for exact laser addressing of the ions. Moreover, in the ATIQ project [193] waveguides made of AlN (aluminum nitride) as well as splitters and optical switches for integrated light management will be investigated and included into the bottom wafer of a 3D ion trap.

iii) With an increasing number of electrodes, also the control electronics and the corresponding on-chip wiring as well as connections to the external voltage sources becomes more complex. Thus, the integration of electrode control circuitry is necessary to further increase the number of ions needed for a fault-tolerant quantum computer. Within the PIEDMONS project [143], cryogenic DACs were developed [37] and investigations on integrated switches were performed to be able to connect and disconnect the trap electrodes from the corresponding DACs [194].

All together, this work and the proposed next steps offer a viable roadmap for advancing the state-of-the-art of trapped-ion quantum computing and will help realize useful applications within this field.

Chapter 7

Summary and Outlook

In this work we presented the design, fabrication, and characterization of two microstructured ion traps. The goal of the presented work was to demonstrate a route towards scaling up the number of trapped ions for meaningful use as a quantum information processor. This work applies industrial microfabrication technologies to the production of microstructured ion traps, where fabrication was carried out in the industrial cleanroom facilities of Infineon Technologies Austria, providing a wide toolpark of microfabrication processes combined with detailed process control.

One approach for scaling to hundreds or more ions is realizing a 2D ion trap array architecture, in which ions are confined in an array of individual trapping sites. A possible minimal-instance design aiming for two parallel 1D arrays of ion traps was successfully fabricated and assembled for operation in the experiment. In order to realize the complex trap layout, a multi-metal layer technology was applied, which allows the routing of electrodes in lower lying metal layers. Electrical functionality was verified by measurements of metal and via resistance, breakdown voltage, and trap capacitance. Trapping of single ions in individual trapping sites of the trap array was shown and shuttling along the 1D array was successfully conducted. However, characterization in the ion trap experiment revealed relatively high heating rates in the range of $100 - 500\,\mathrm{q/s}$. Preliminary results of a second version of the ion trap with a change in electrode material from AlSiCu to Au and a recess of the gap oxide between electrodes suggest a reduction of these values by around one order of magnitude and require further investigations to discriminate technical noise from surface electric field noise. Moreover, the ion trap layout was adapted due to observed charge-carrier effects induced in the silicon substrate and an oscillating magnetic field. The oscillating B-field was caused by the high trap capacitance. Both of these issues could be solved by the layout modification. At the time of writing this thesis, a further investigation of the new

iteration of the 2D twin trap is being carried out, with focus on ion coupling between the 1D arrays by tuning the amplitude of the RF electrode in between the two ion chains. Coupling of ions in both lattice directions allows for a maximum lattice connectivity and thus forms an important step towards a quantum information processor.

Furthermore, a second microstructured ion trap with an increased confinement potential of 1 eV was developed and presented in this thesis. To achieve such a high trap depth in microstructured ion traps, a 3D architecture is required. The ion trap was manufactured with the help of MEMS technology in the industrial cleanroom facility of Infineon. The design of the trap is based on three wafers: a bottom surface trap, a glass spacer, and a top wafer with two additional DC electrodes. These wafers are structured individually and subsequently anodically wafer bonded to form the 3D architecture that creates the deep confinement potential. Due to the additional DC electrodes in the top layer, which initially do not carry any RF voltage, we refer to this trap as a hybrid trap. The structural properties of the device was extensively tested by electrical measurements and surface analysis, and the successful wafer bond was verified by analysis of the depletion zone, die-shear tests and scanning acoustic microscopy. The performance during ion trap operation was investigated by colleagues in the TIQI group at ETH Zürich. The characterization revealed relatively low axial heating rates of 40 q/s at cryogenic temperatures, but a high micromotion of the axial mode. We suspect the cause of this micromotion to be stray electric fields generated by the unshielded sidewalls of the glass spacer. In future iterations of this trap, a metal coating on these sidewalls could help reducing stray fields induced by stray charges on exposed dielectric materials. Moreover, similar as with the 2D twin trap, an undesired oscillating magnetic field caused by charging currents of the trap capacitance of 53 pF was observed. In general, a change of the substrate material from silicon to an insulator such as fused silica or sapphire would circumvent the need for a shield layer, leading to a significant reduction of the trap capacitance and the associated limitations during trap operation. Due to the manufacturing of the trap based on industrial MEMS technologies and the thus achieved high trap depth through a 3D architecture shows a promising direction towards stable, microfabricated ion traps, which are scalable to a large number of ions.

Finally, an approach to combine the two trap designs of the 2D ion trap array and the hybrid ion trap with increased confinement potential was given. Adding a top layer and introducing a vertical separation of DC and RF electrodes allows for scaling up the ion trap to individually trap hundreds of ions without being limited by an extraordinary high RF voltage or a decreased trap depth. The ion trap concept presented is compatible with a production based on CMOS and MEMS technologies, thus enabling the integration of additional functionality such as integrated electronics

(digital-to-analog converters, switches) or optics (waveguides) that support further scaling. In general, the miniaturization of the ion trap and the associated tools and components required for its operation is needed if a universal quantum computer based on thousands or tens of thousands of trapped ions is to be realized. For this reason, the results of this work and the further pursuit of industrially manufactured ion traps are an important step for the development of a useful trapped-ion quantum computer and potential applications.

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